FIG. 1

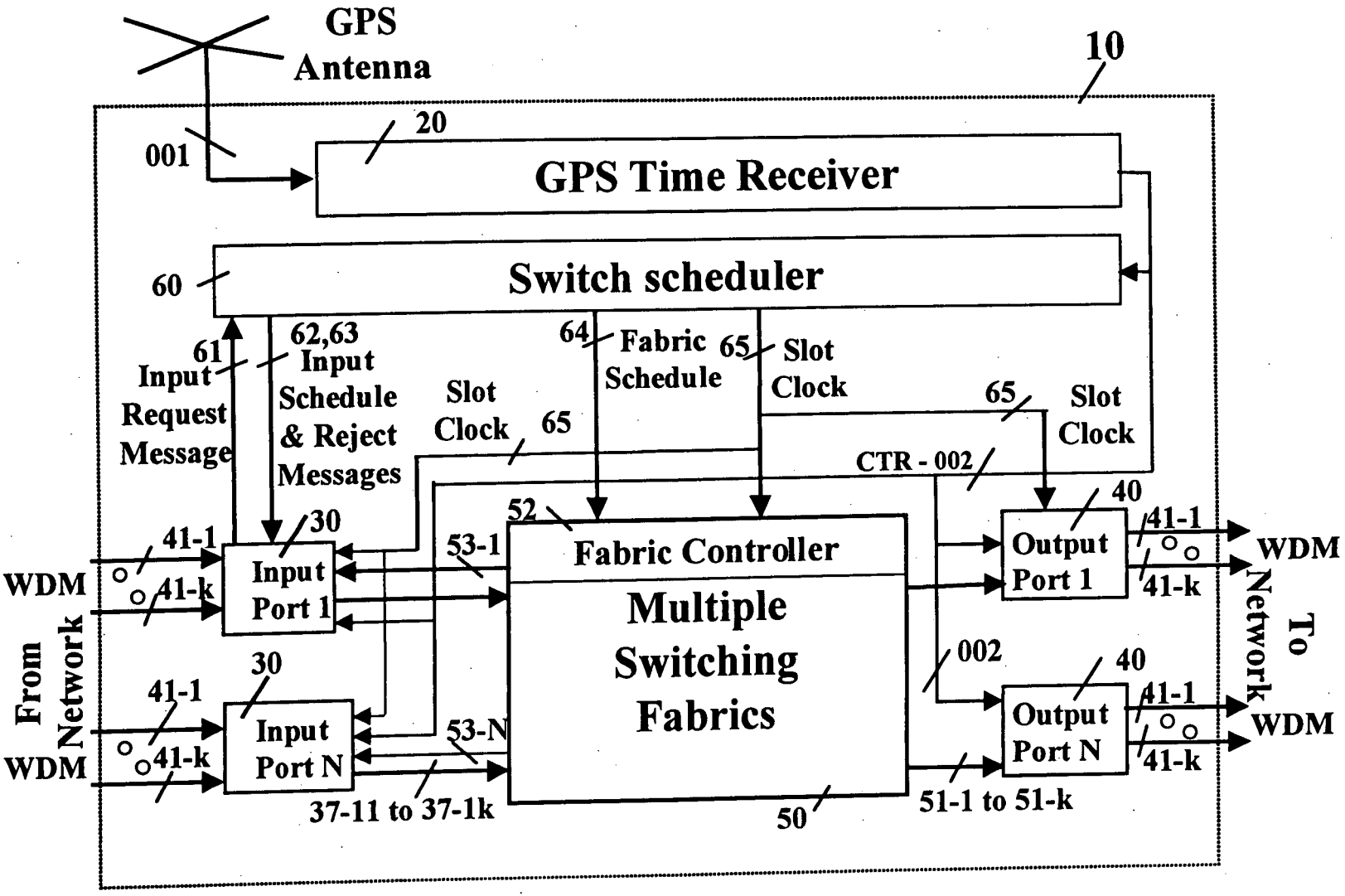


FIG. 2

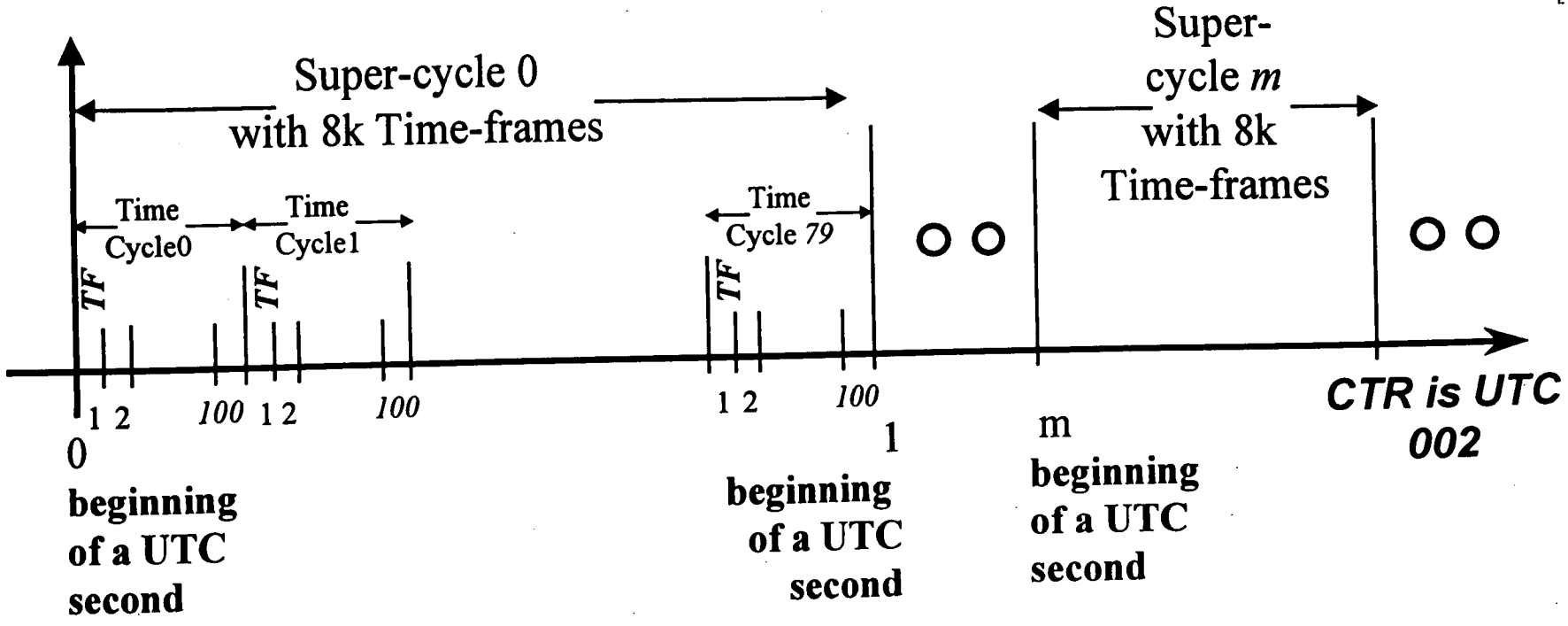


FIG. 3

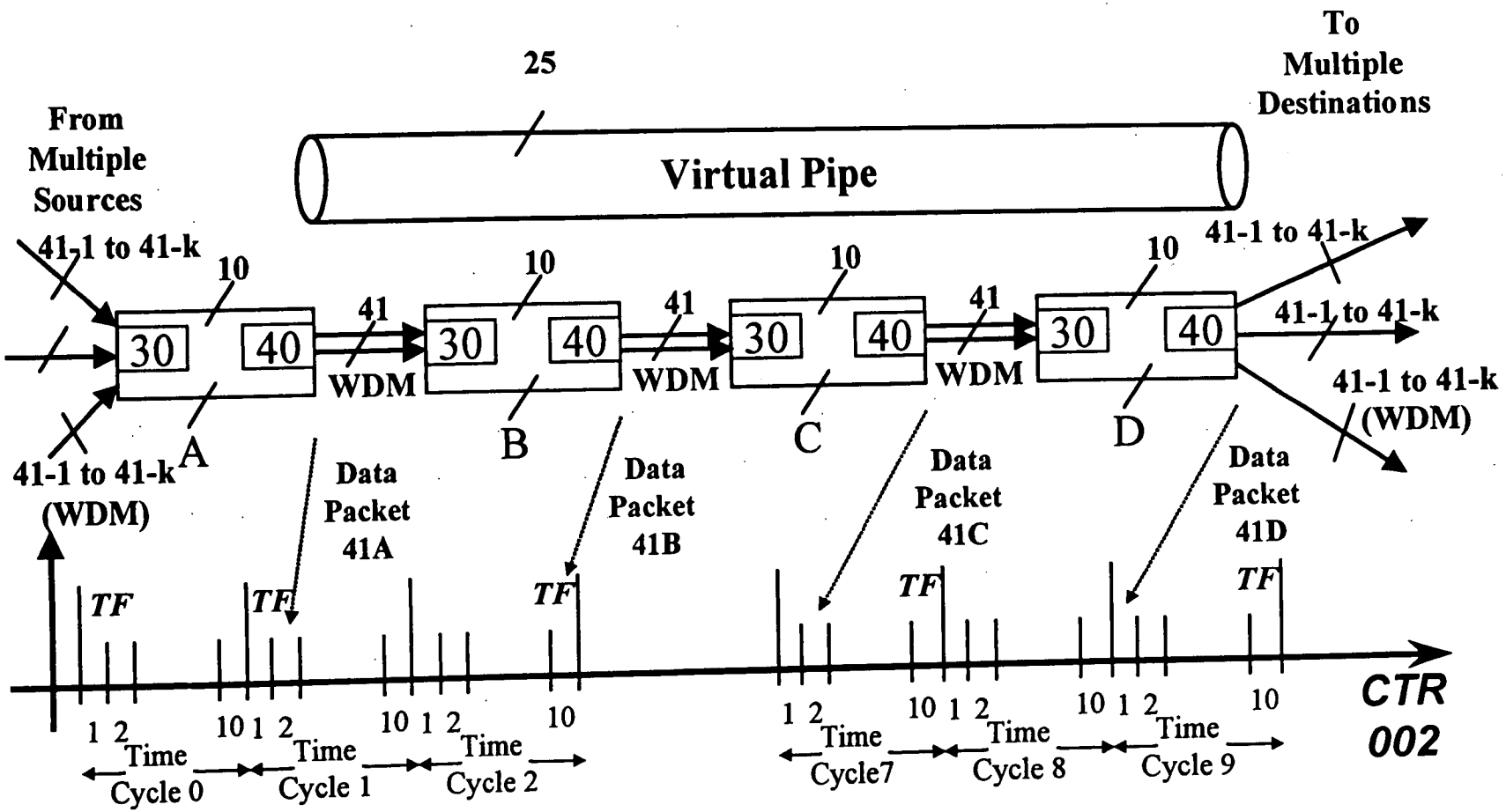


FIG. 4

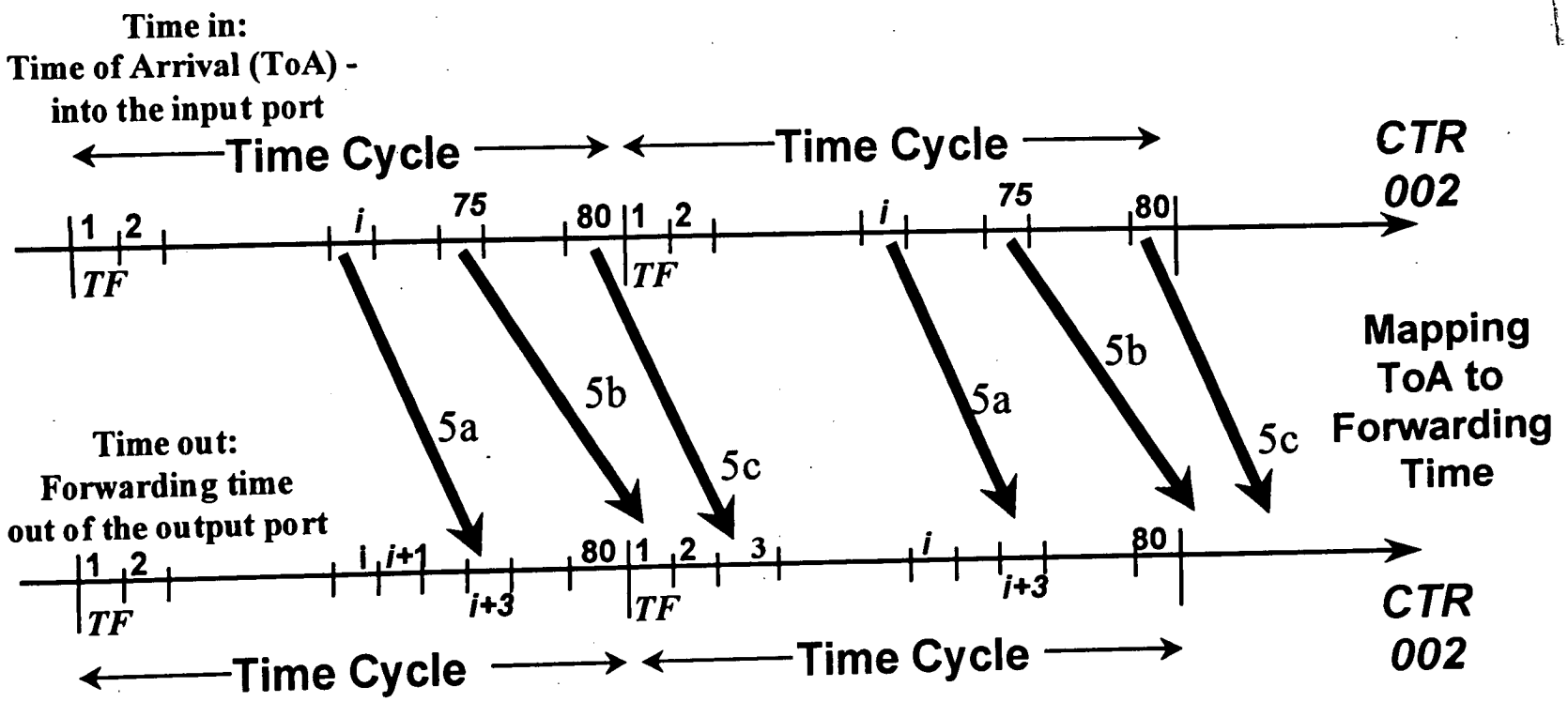
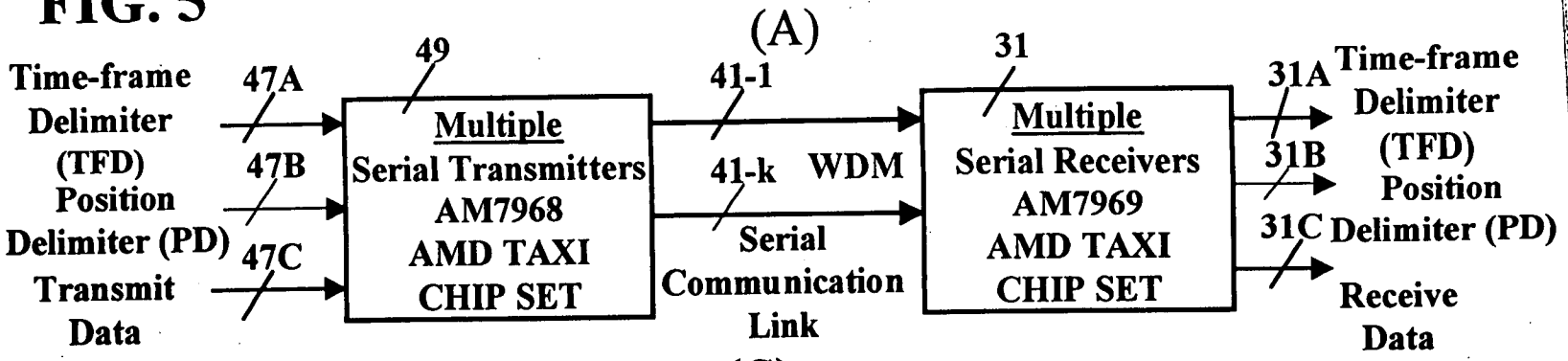


FIG. 5



(B)

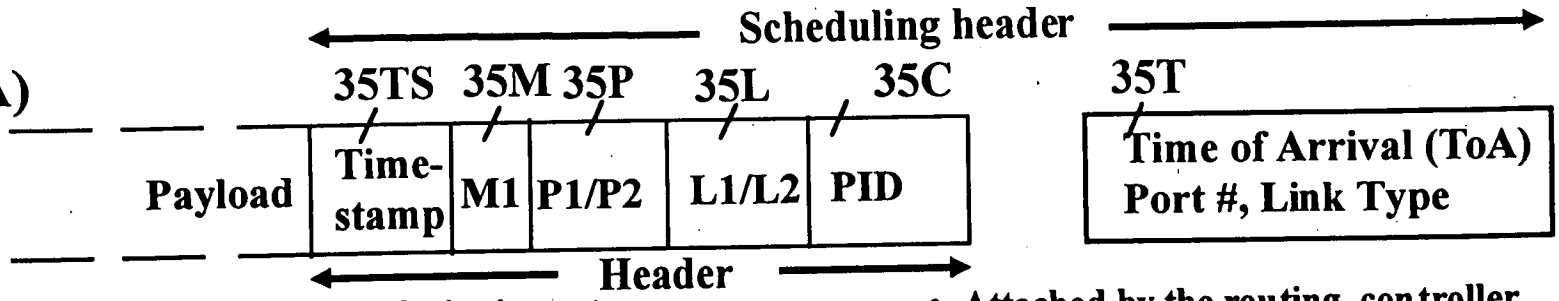
4B/5B encoding scheme		
HEX DATA	4-bit Binary Data	5-bit Encoded Data Codeword
0	0000	11110
1	0001	01001
2	0010	10100
3	0011	10101
4	0100	01010
5	0101	01011
6	0110	01110
7	0111	01111
8	1000	10010
9	1001	10011
A	1010	10110
B	1011	10111
C	1100	11010
D	1101	11011
E	1110	11100
F	1111	11101

(C)

4B/5B encoding scheme		
Control Input		10-bit Encoded Control Codeword
HEX DATA	Binary Data	
1	0001	11111 11111
2	0010	01101 01101
3	0011	01101 11001
4	0100	11111 00100
5	0101	01101 00111
6	0110	11001 00111
7	0111	11001 11001
8	1000	00100 00100
9	1001	00100 11111
A	1010	00100 00000
B	1011	00111 00111
C	1100	00111 11001
D	1101	00000 00100
E	1110	00000 11111
F	1111	00000 00000

FIG. 6

(A)



35TS is given at:
(1) the source, and/or
(2) the sub-network boundary

- Attached by the routing controller
- The TOA represent the instant value of the common time reference 002 when the packet is arrived to the input port

(B) P1/P2, M1, L1/L2 values

P1/P2=00 -CBR – constant bit rate; scheduled data packet P1/P2=01 -VBR – variable bit rate; scheduled data packet P1/P2=10 -"Best Effort"; non-scheduled data packet P1/P2=11 - Rescheduled data packet
M1=0 - point-to-point packet (one destination) M1=1 - multicast packet (multiple destinations)
L1/L2=00 - first data packet location in the flow - compute a schedule L1/L2=01 - middle data packet location in the flow - same as previous schedule L1/L2=10 - last data packet location in the flow - same as previous schedule L1/L2=11 - decode packet address and schedule it regardless of its location

FIG. 7

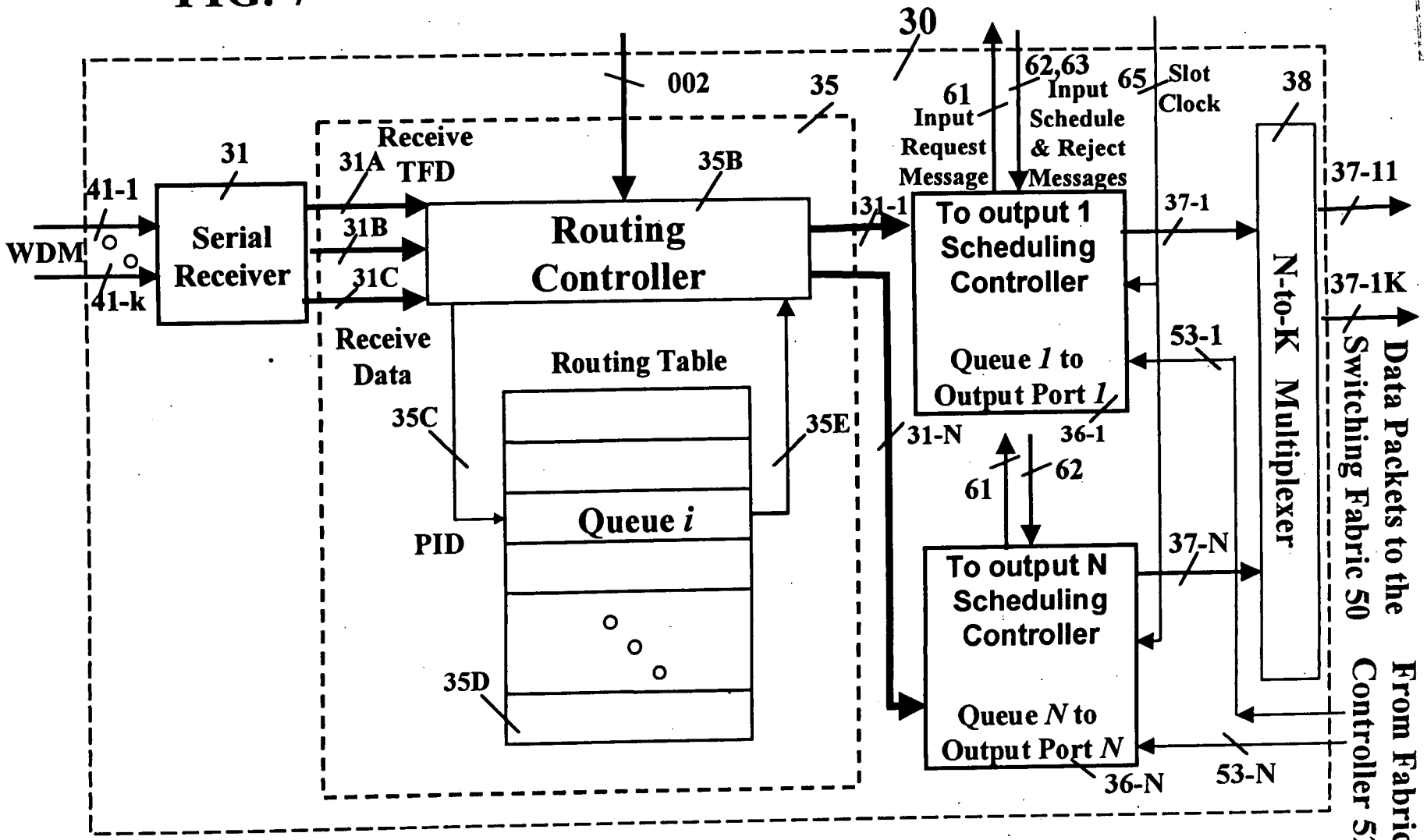


FIG. 8

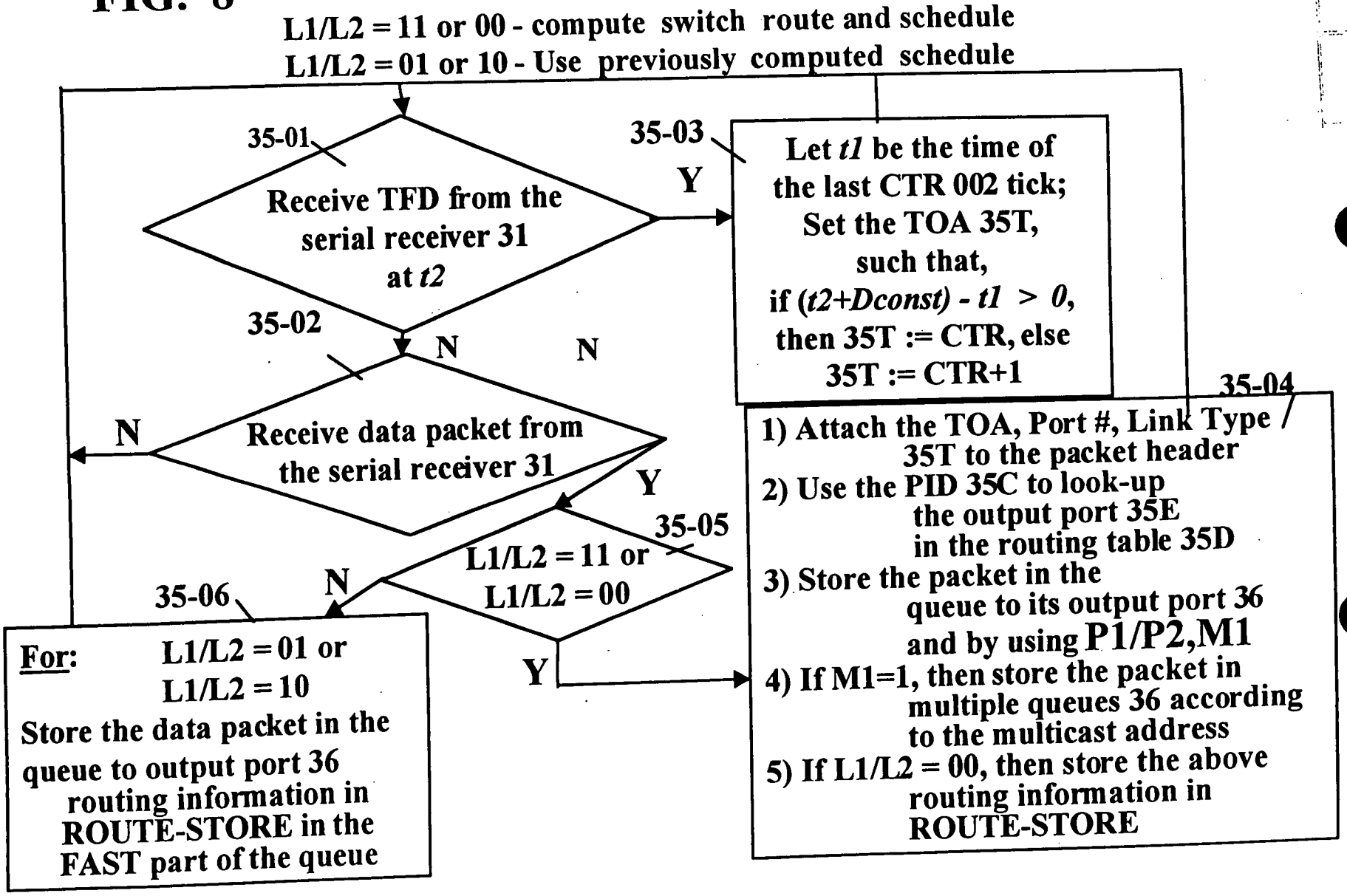


FIG. 9

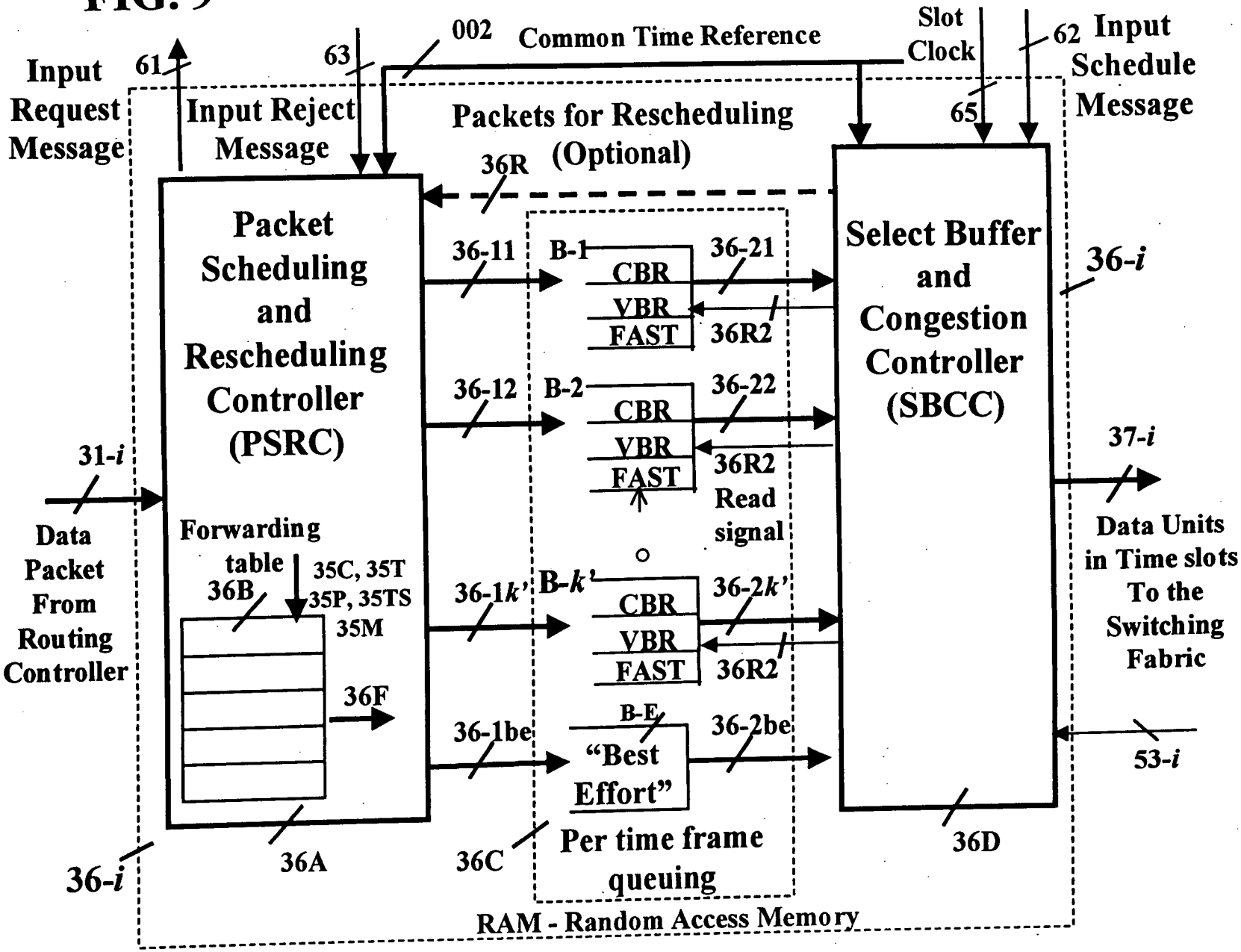


FIG. 10

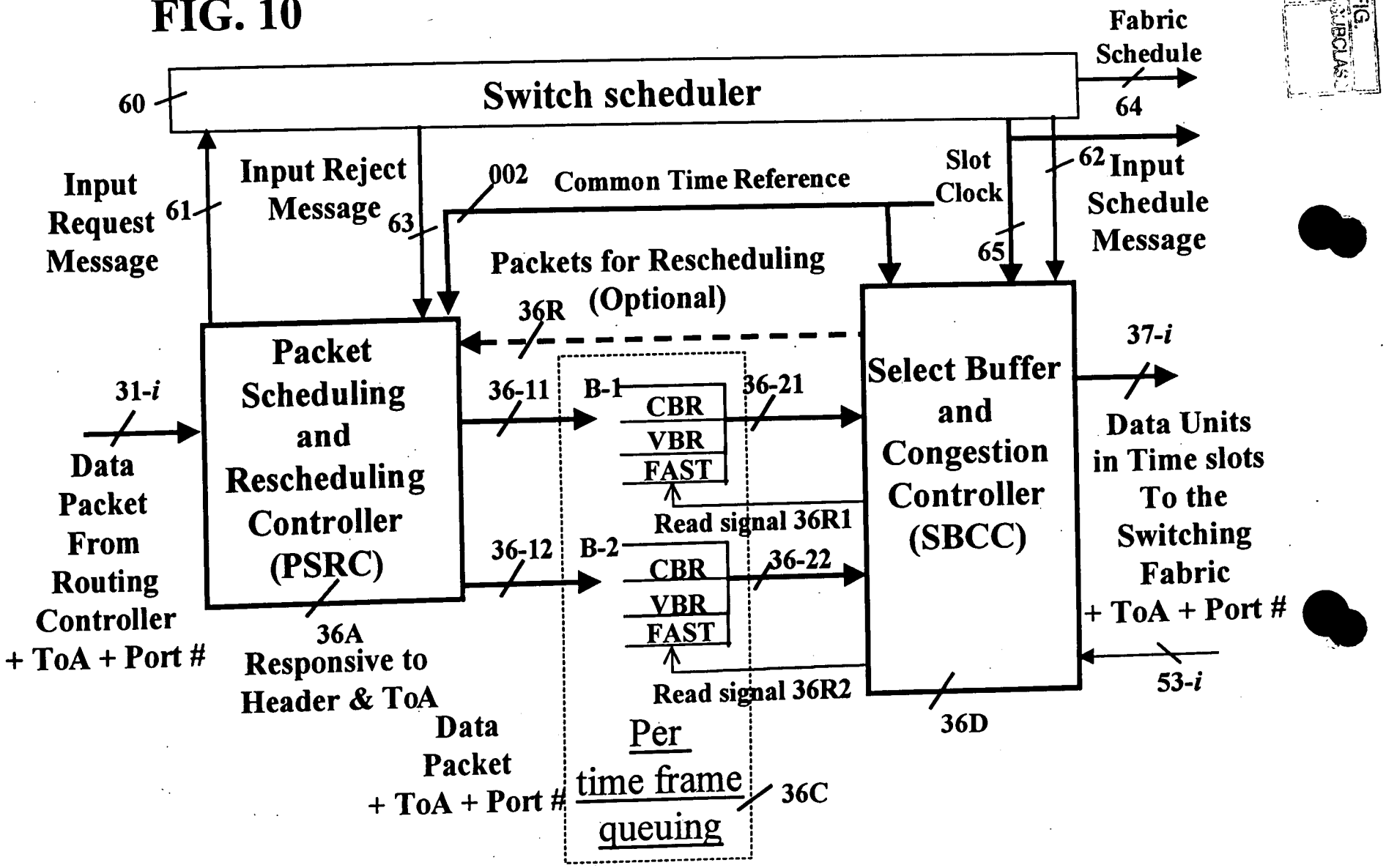


FIG. 11

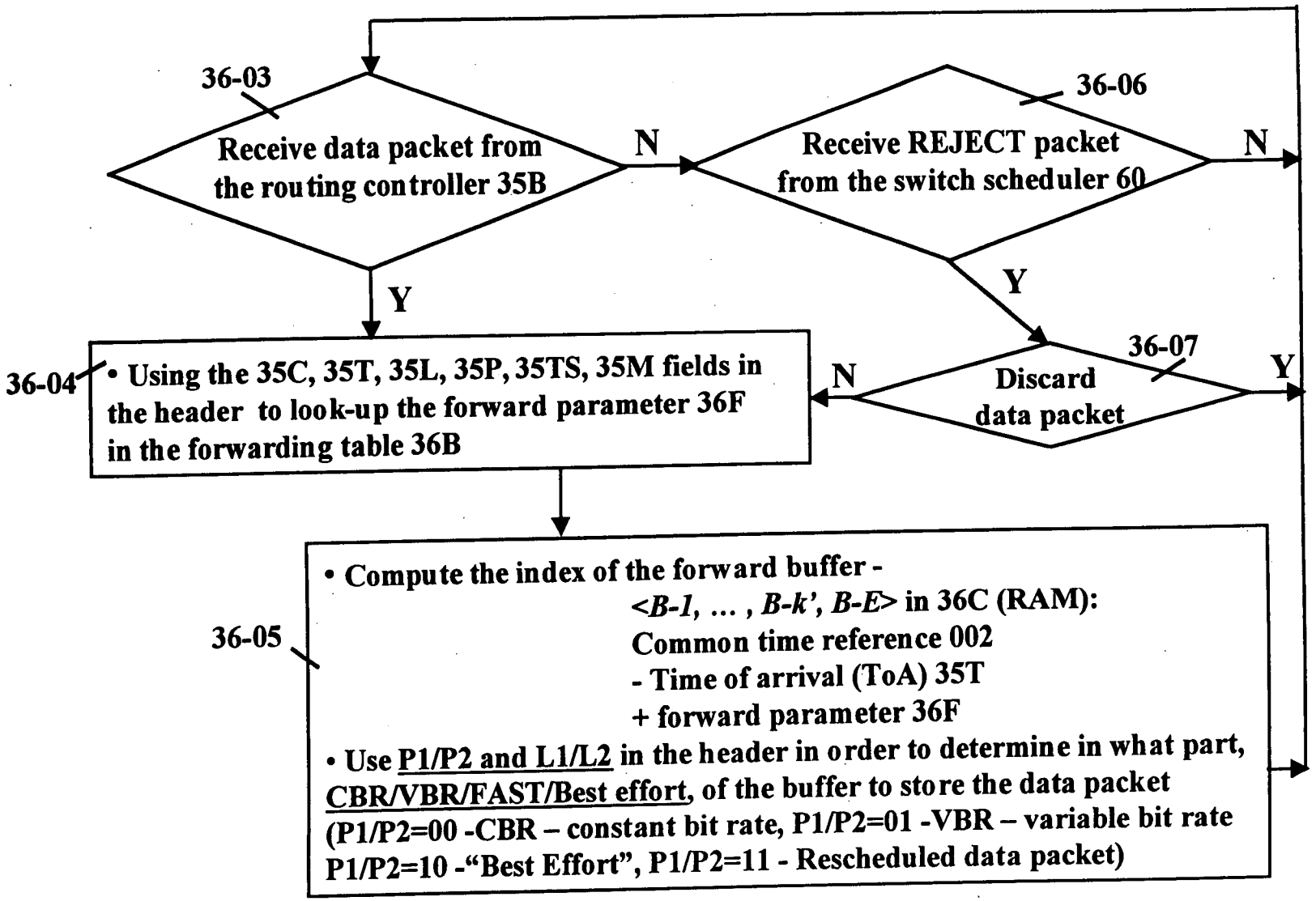

36-03
Receive data packet from the routing controller 35B
N
36-06
Receive REJECT packet from the switch scheduler 60
N
Y
Y
36-07
Discard data packet
N
Y
36-04
• Using the 35C, 35T, 35L, 35P, 35TS, 35M fields in the header to look-up the forward parameter 36F in the forwarding table 36B
36-05
• Compute the index of the forward buffer - <B-1, ... , B-k', B-E> in 36C (RAM):
Common time reference 002
- Time of arrival (ToA) 35T
+ forward parameter 36F
• Use P1/P2 and L1/L2 in the header in order to determine in what part, CBR/VBR/FAST/Best effort, of the buffer to store the data packet
(P1/P2=00 -CBR – constant bit rate, P1/P2=01 -VBR – variable bit rate
P1/P2=10 -"Best Effort", P1/P2=11 - Rescheduled data packet)

FIG. 12

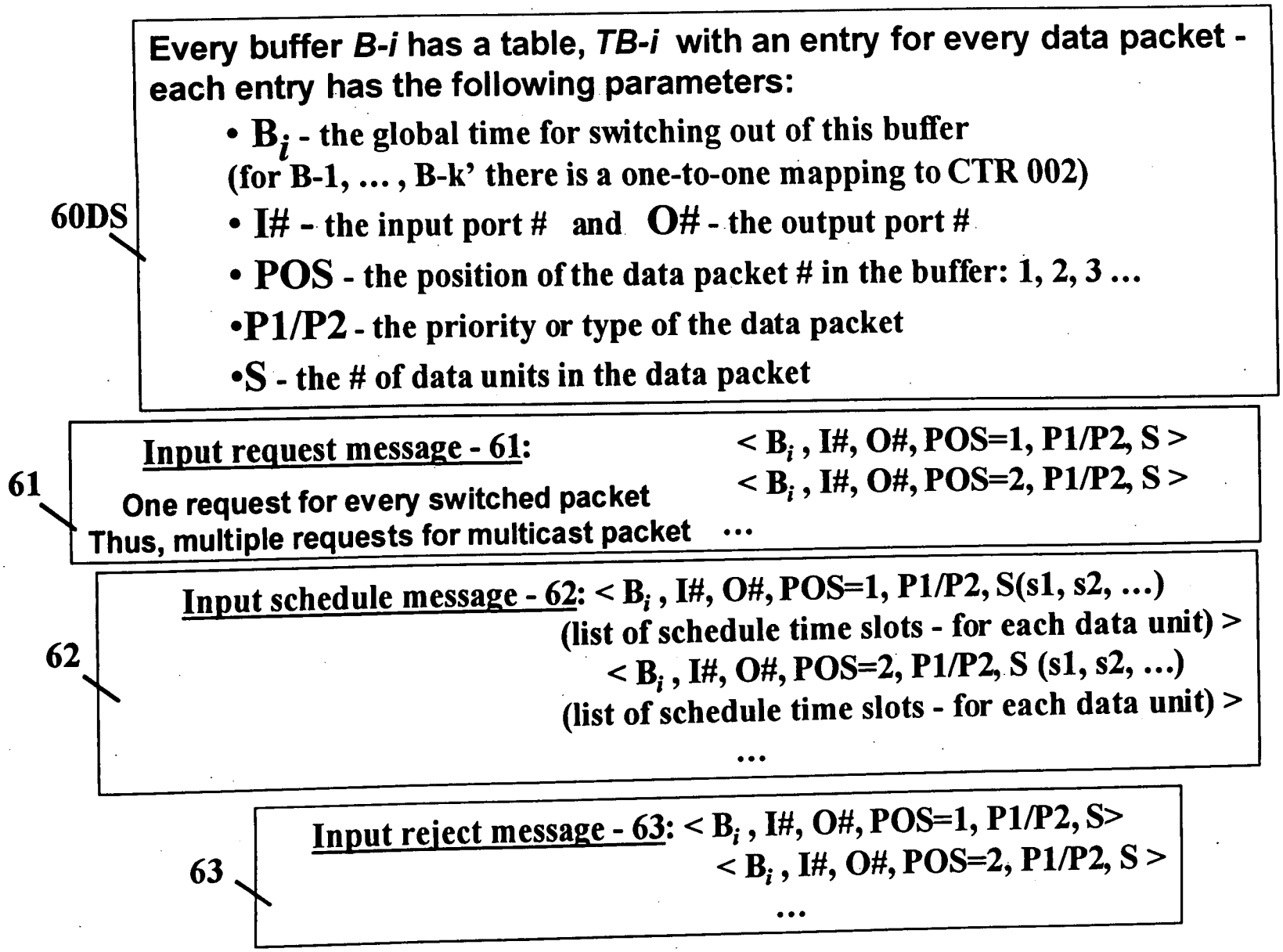


FIG. 13

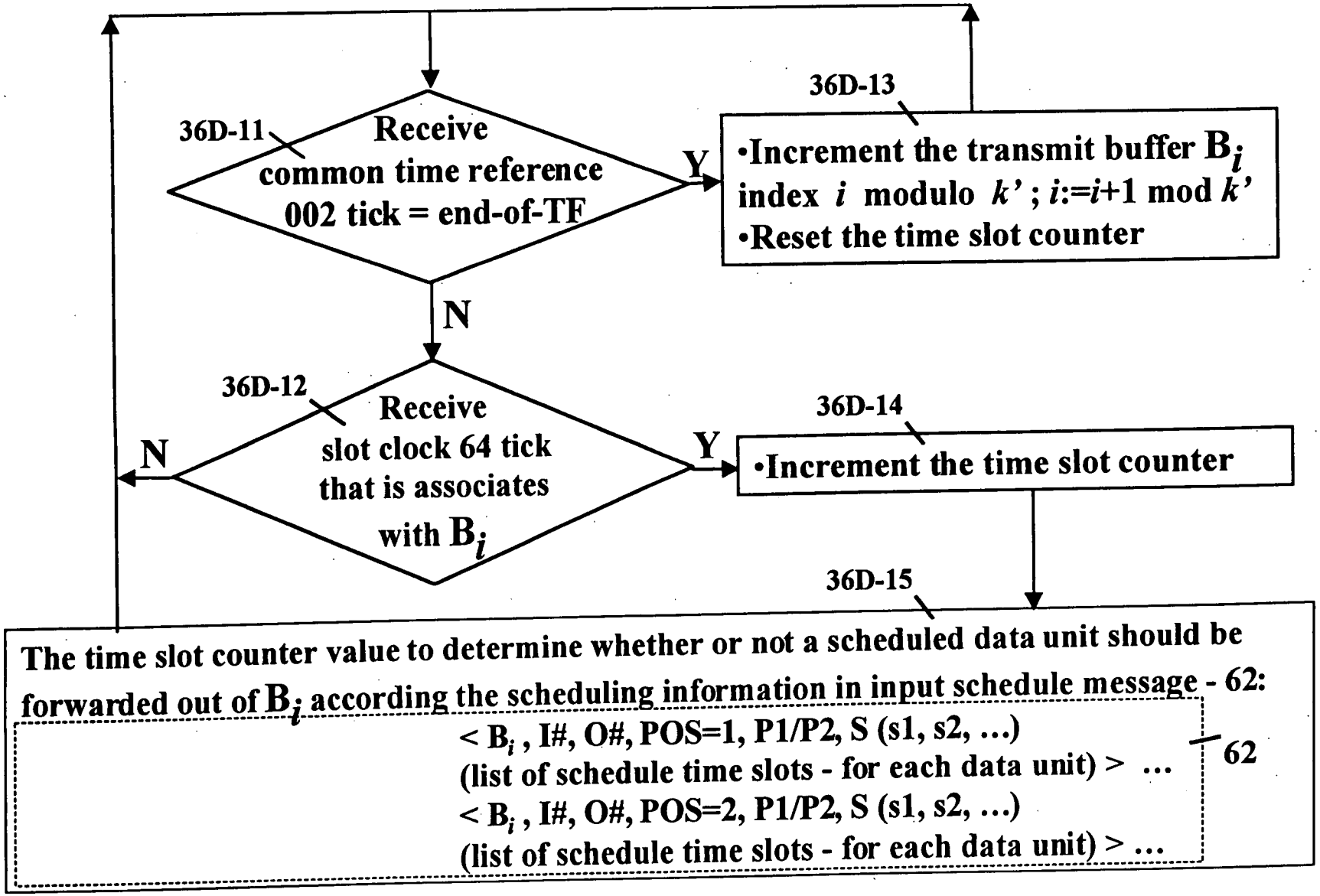


FIG. 14

The following phases - typically, each phase takes one time frame (TF):

<table>
<tr><td colspan="2">Phase 1) TF(t) - receive data packet,
route (FIG. 8, computation steps 35-01 to 35-04), and
schedule (FIG. 11, computation steps 36-03 to 36-07)</td></tr>
<tr><td>Phase 2) TF(t+1) - the packet scheduling and rescheduling controller 36A sends an input request message 61 (FIG. 12) to switch scheduling controller 60. The switch scheduling controller 60 computes the schedule and returns input schedule message 62 to the select buffer and congestion controller 36D.</td><td>Possibly more times for rescheduling of: VBR, MCST (multicast) and "Best Effort) - after receiving Input reject message 63</td></tr>
<tr><td colspan="2">Phase 3) TF(t+2) - The select buffer and congestion controller 36D forwards the data units to the output port 40 via switching fabric 50 according to the input schedule message 62</td></tr>
<tr><td colspan="2">Phase 4) TF(t+3) - The output port 40 forward the data packet received during TF(t+2) via the serial transmitter 49.</td></tr>
</table>

FIG. 15

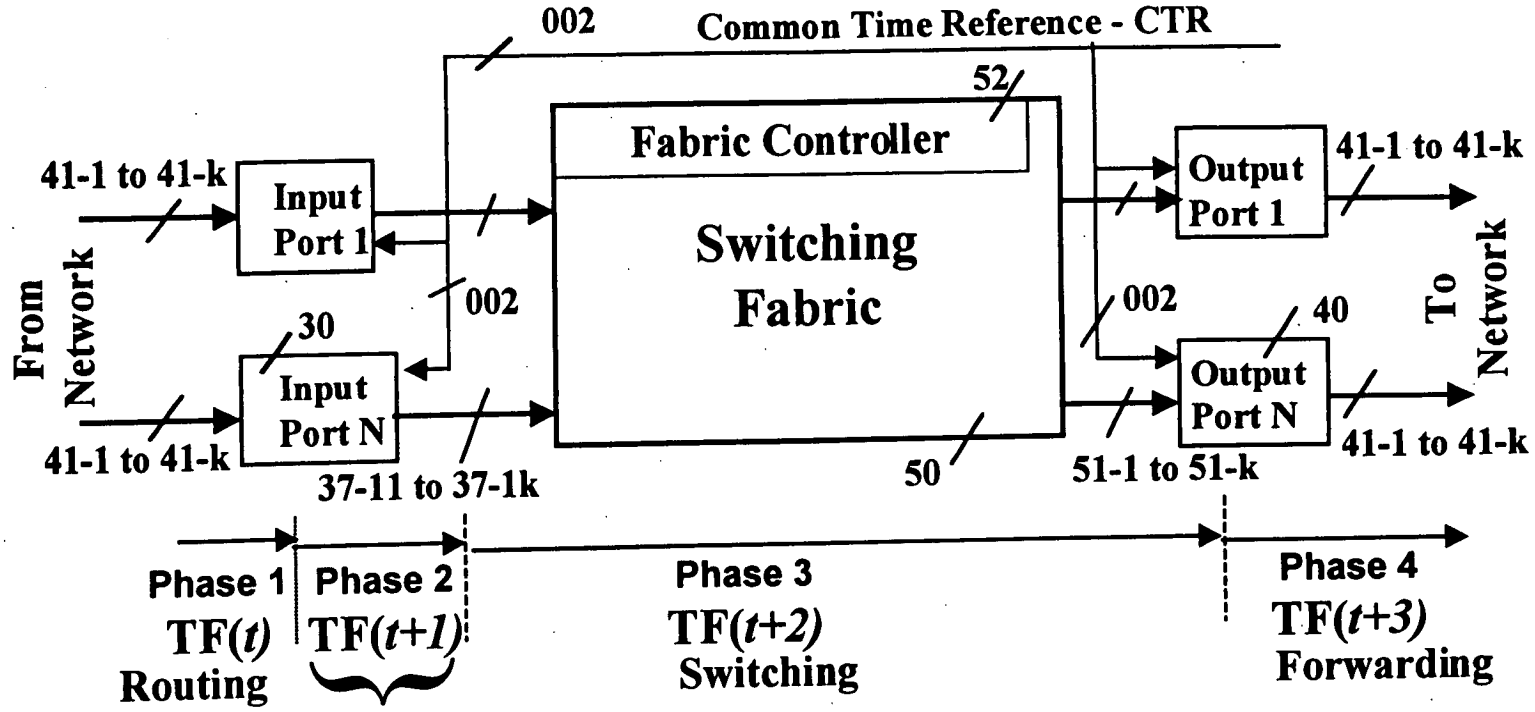
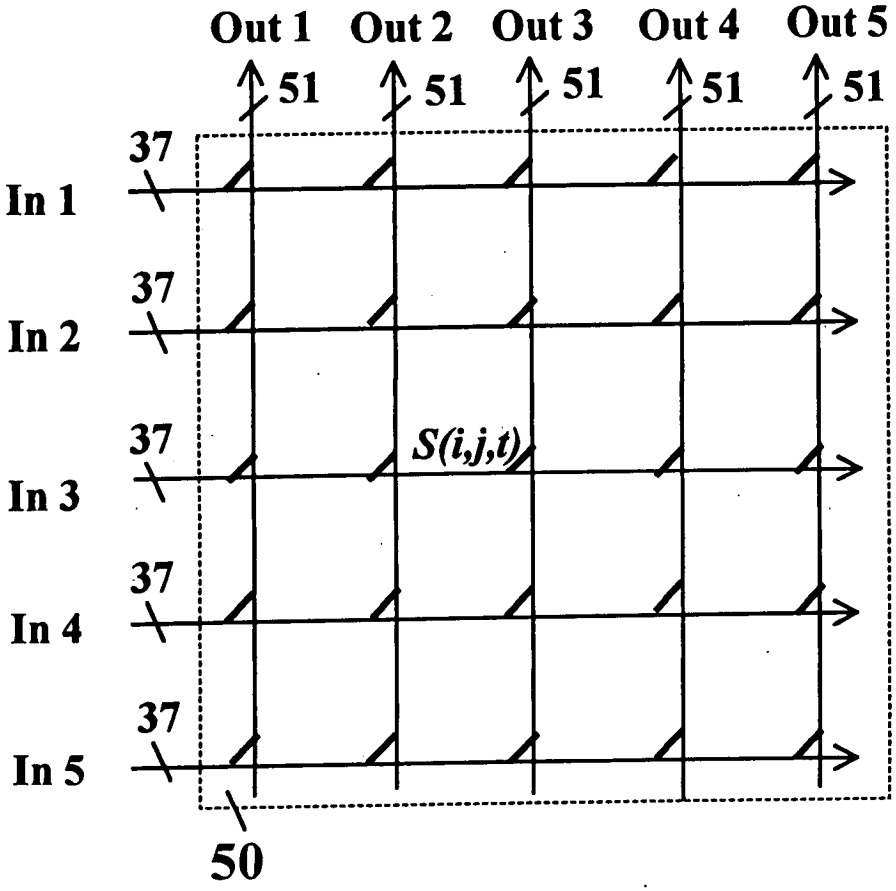

002
Common Time Reference - CTR
52
Fabric Controller
Switching Fabric
41-1 to 41-k
Input Port 1
From Network
30
Input Port N
41-1 to 41-k
002
37-11 to 37-1k
50
Output Port 1
41-1 to 41-k
002
40
Output Port N
To Network
51-1 to 51-k
41-1 to 41-k
Phase 1
TF(t)
Routing
Phase 2
TF(t+1)
Phase 3
TF(t+2)
Switching
Phase 4
TF(t+3)
Forwarding
Scheduling and possibly more TFs for rescheduling of: VBR and "Best Effort) - after receiving Input reject message 63

FIG. 16

Switching operation:
(use the fabric schedule message 64, which is the union of all input schedule messages 62)
At time slot 65 *t* in which *S(i,j,t)=1:*
Input port *i* will be connected to output port *j*



Fabric controller:

S(i,j,t) **- switching matrix for every time slot 65 *t* (in each time frame, time cycle and super cycle) - see FIG. 27, the matrix defines which input *i* should be connected to output *j*.**

- **1. At every time slot an input port can be connected to one or more output ports (multicast - MCST)**
- **2. At every time slot an output port can be connected to at most one input port (this can be relaxed if needed)**

FIG. 17

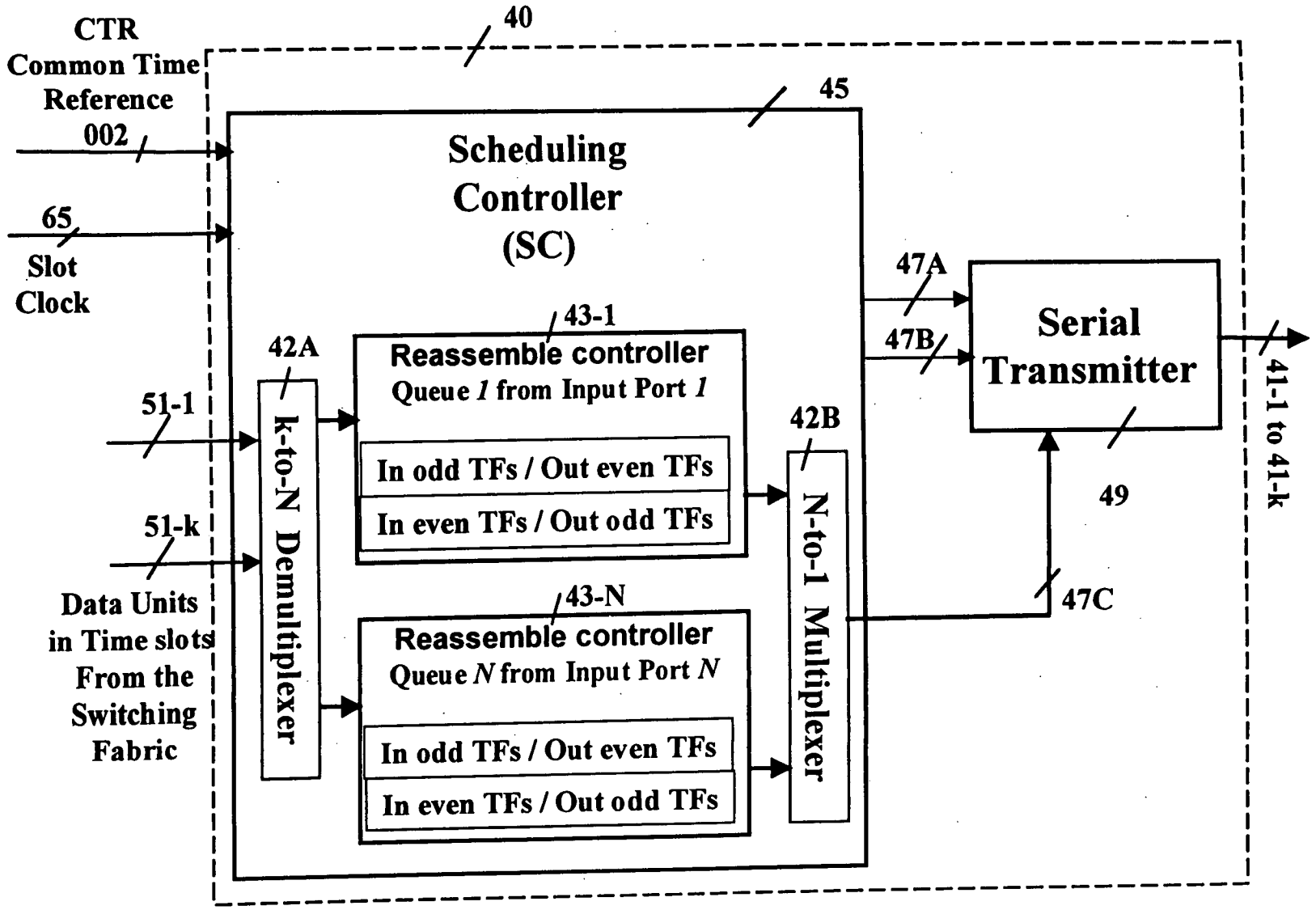


FIG. 18

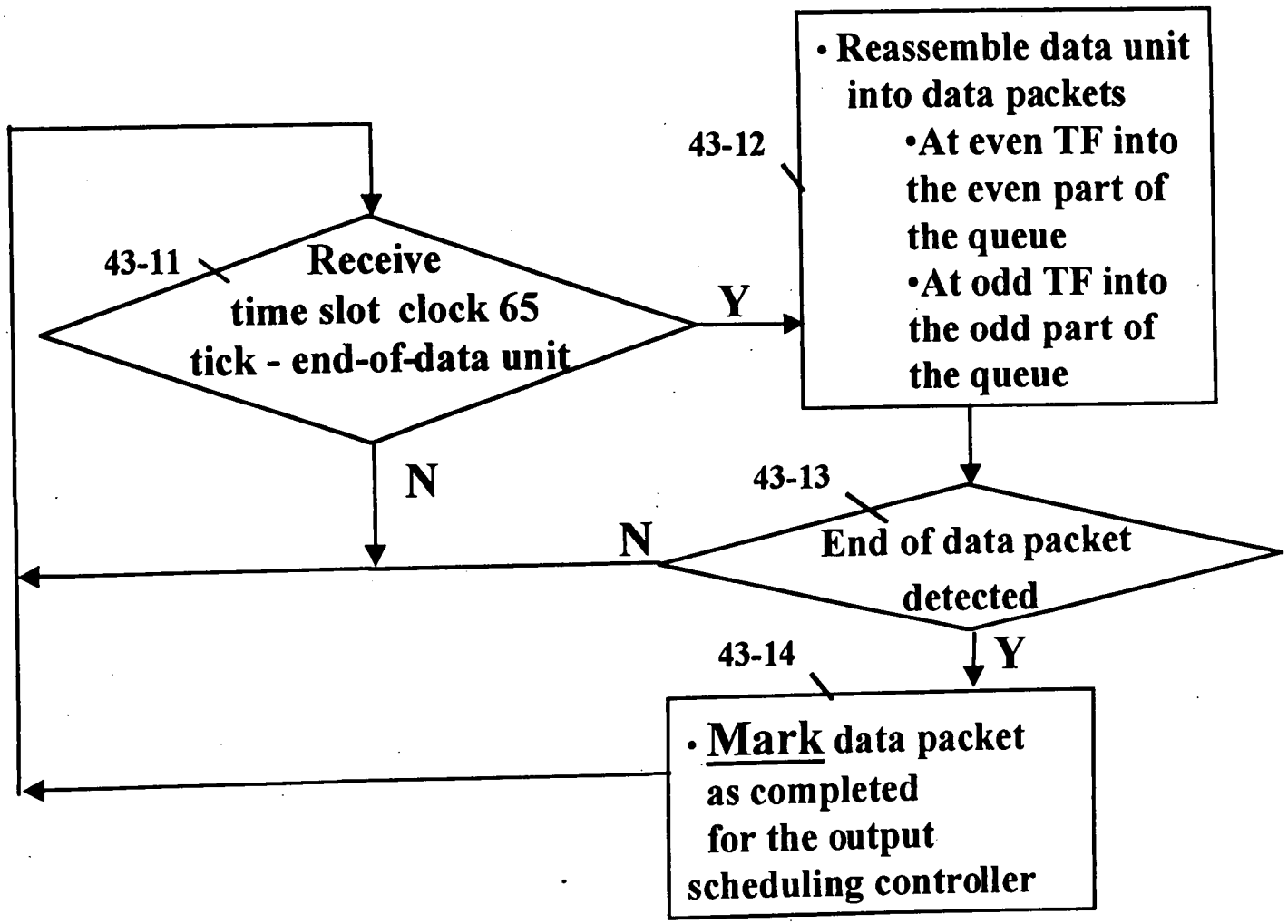


FIG. 19

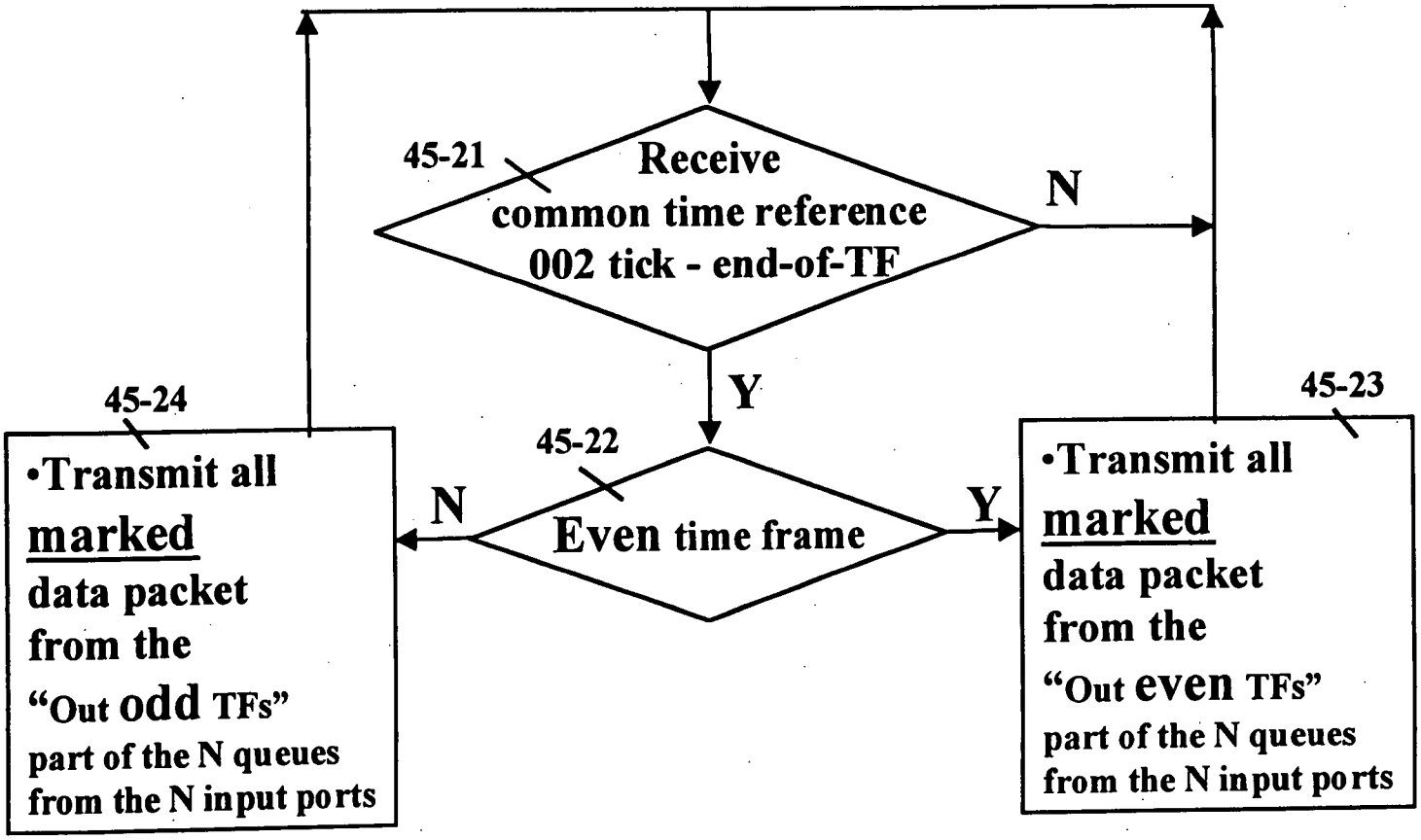


FIG. 20

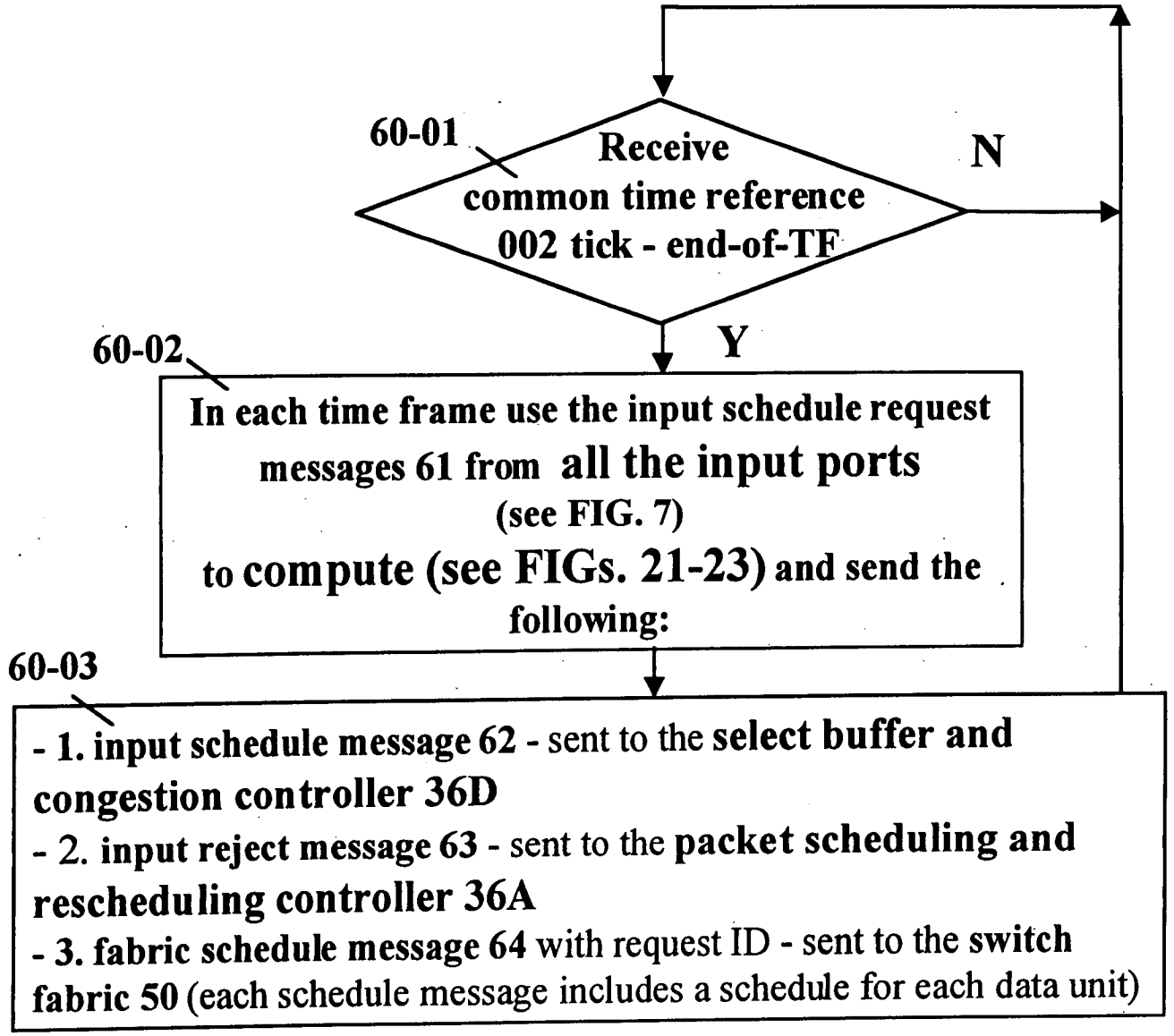


FIG. 21

there are n slots for scheduling the transfer through the fabric of N data units in a time frame: n=>N

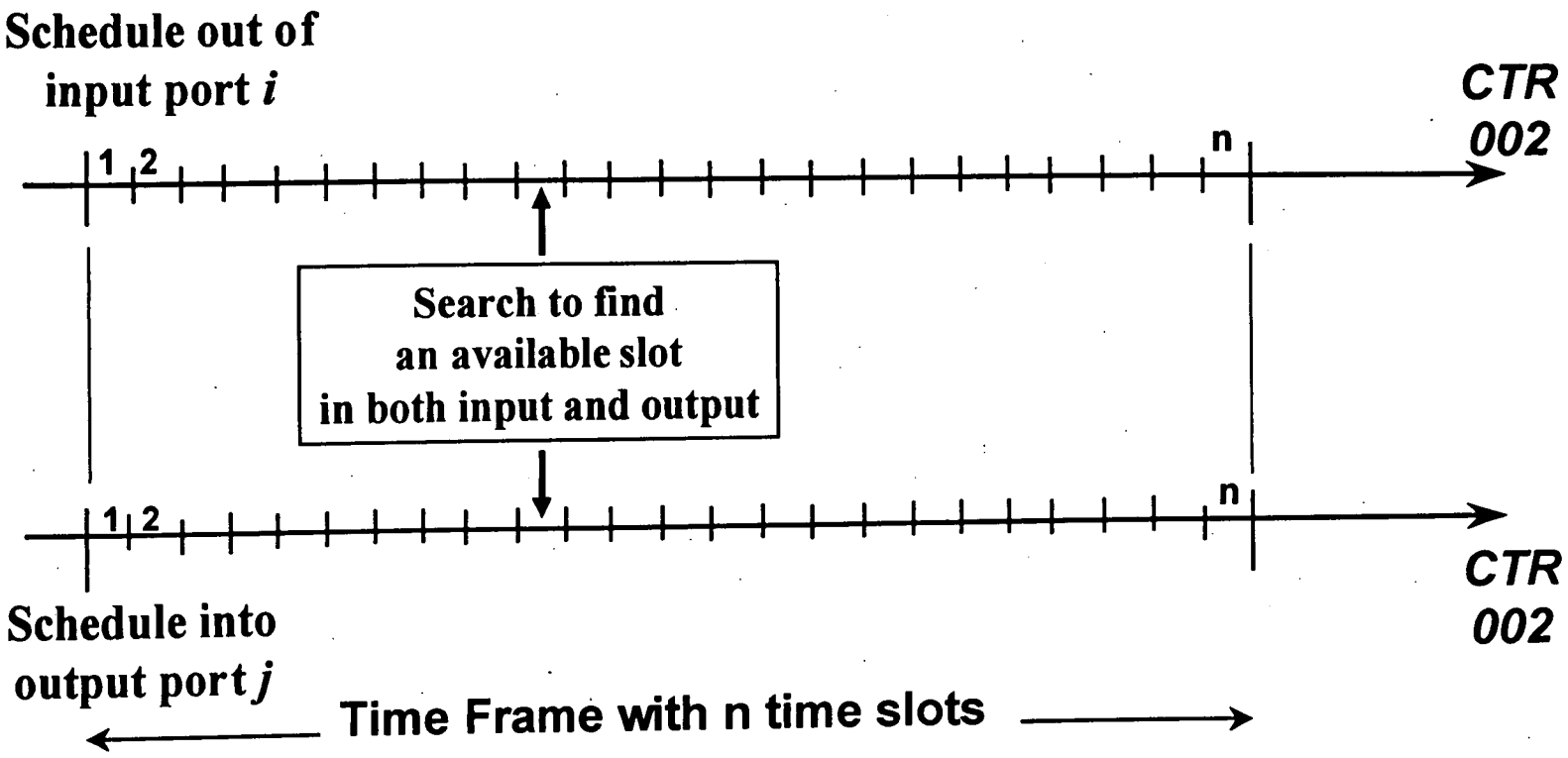


FIG. 22

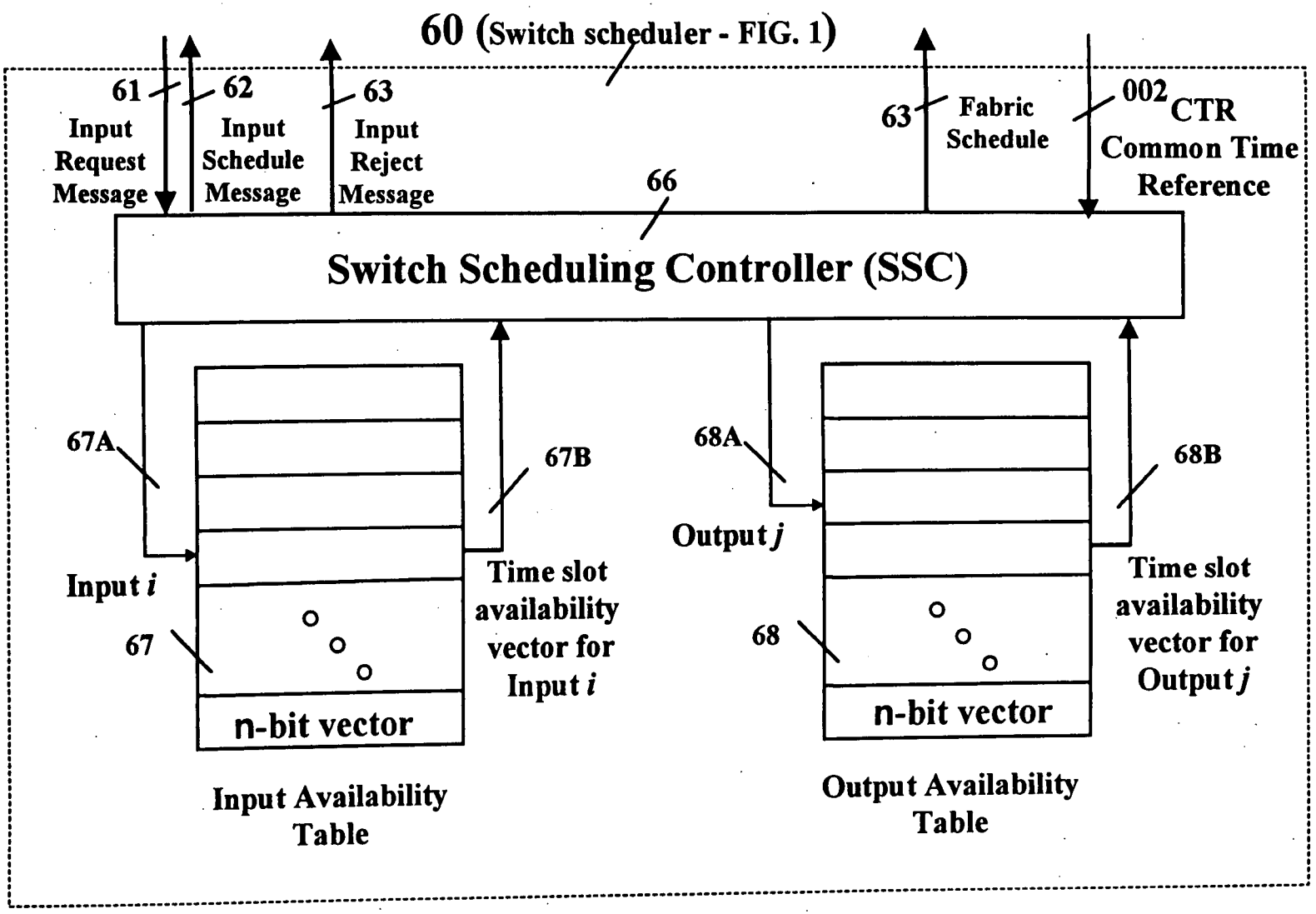


FIG. 23

Compute schedule for each data unit in the:

60-10

61

Input request message - 61: $< B_i$, I#, O#, POS=1, P1/P2, S >

$< B_i$, I#, O#, POS=2, P1/P2, S >

One request for every switched packet Thus, multiple requests for multicast packet

Given:

For TF(*t+1*) there are two vectors size *n* (slots) for switching from input to output:

I[*t,s*] *(1<= s <= n) for* the input port, and

O[*t,s*] *(1<= s <= n)* for the output port

Initialization:

At the beginning of the schedule computation of each time frame: I[*t,s*] = O[*t,s*] = 0 *(1<= s <= n)*

Compute:

For slot *s=1 to n* find the first slot that is available in both I[*t,s*] = 0 and O[*t,s*] = 0, then DO:

- I[*t,s*] = O[*t,s*] := 1
- *s* is the slot number in which the data unit should be transferred from input, I#, to output, O#, through the fabric 50

FIG. 24

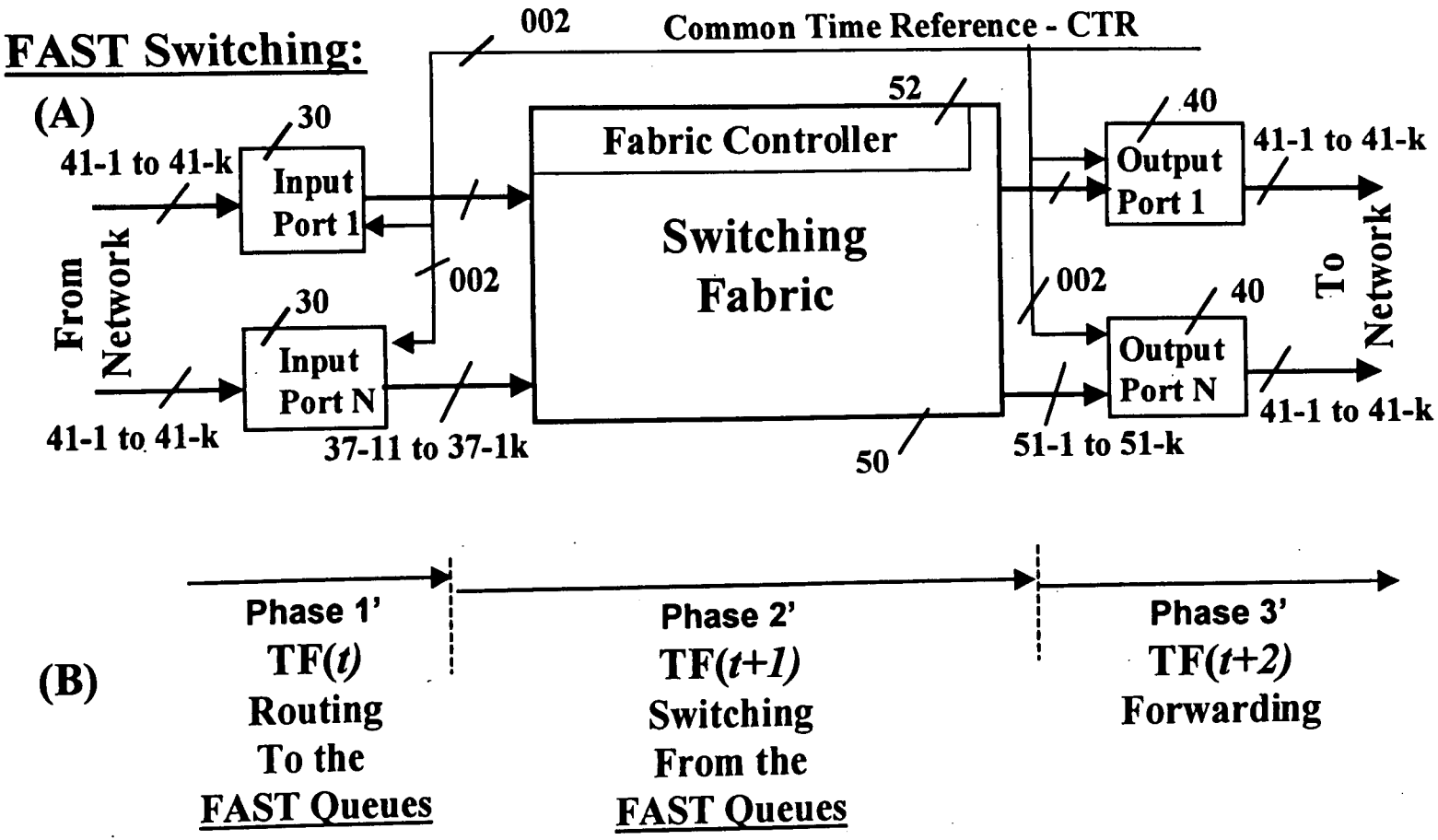


FIG. 25

FAST switching - Fabric controller - switching matrices -

M(i,j,t) - for every time slot:

2510

t - is defined by the triplet:
- *s* - number of slot positions in time frame
- *f* - number of frame positions in time cycle
- *c* - number of cycle positions in super cycle

[Note: total number of switching matrices - *M(i,j,t)* - *s*f*c*]

Matrix *M(i,j,t)*, *such that*, $1 <= t <= s*f*c$:

4 output ports - *j*

4 input ports - *i*

	output-1	*output-2*	*output-3*	*output-4*
input-1				
input-2		*value,type*		
input-3				
input-4				

2500

value=0 - ***dis*connect** input port from output port
value=1 - **connect** input port to output port
type =0 - **temporary value** in this switching matrix
type =1 - **permanent value** in this switching matrix

FIG. 26

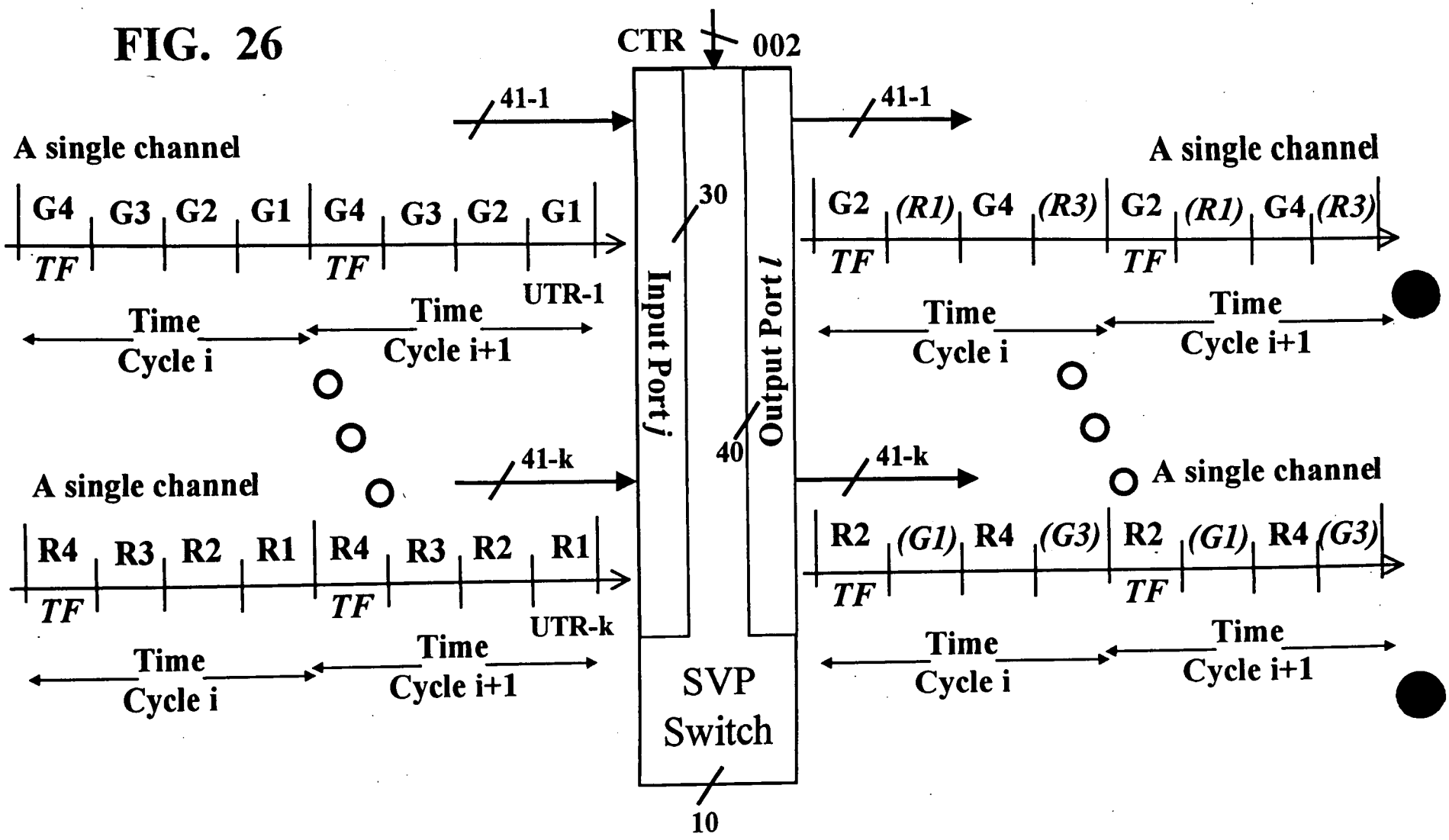


FIG. 27

Mapping: *(p-in,w-in, t-in,c-in)* TO *(p-out,w-out, t-switch, c-switch t-out,c-out)*

2710

p-in - input port #
w-in - input wavelength (color)
t-in - time frame # in (within a time cycle)
c-in - time cycle # in (within a super cycle)

2720

p-out - output port #
w-out - output wavelength (color)
t-switch - time frame # switch (within a time cycle)
c-switch - time cycle # switch (within a super cycle)
t-out - time frame # out (within a time cycle)
c-out - time cycle # out (within a super cycle)

Time frame switching for a given: *p-in*

2700

t-in \ *c-in*	Time Cycle 1	Time Cycle 2		Time Cycle *l*
TF-R1				
TF-R2				
TF-R3		*(p-out,w-out, t-switch,c-switch t-out,c-out)*		
TF-R4				
TF-G1				
TF-G2				
TF-G3				
TF-G4				

"Color" R *w-in* (see FIG. 26)

"Color" G *w-in*

FIG. 28

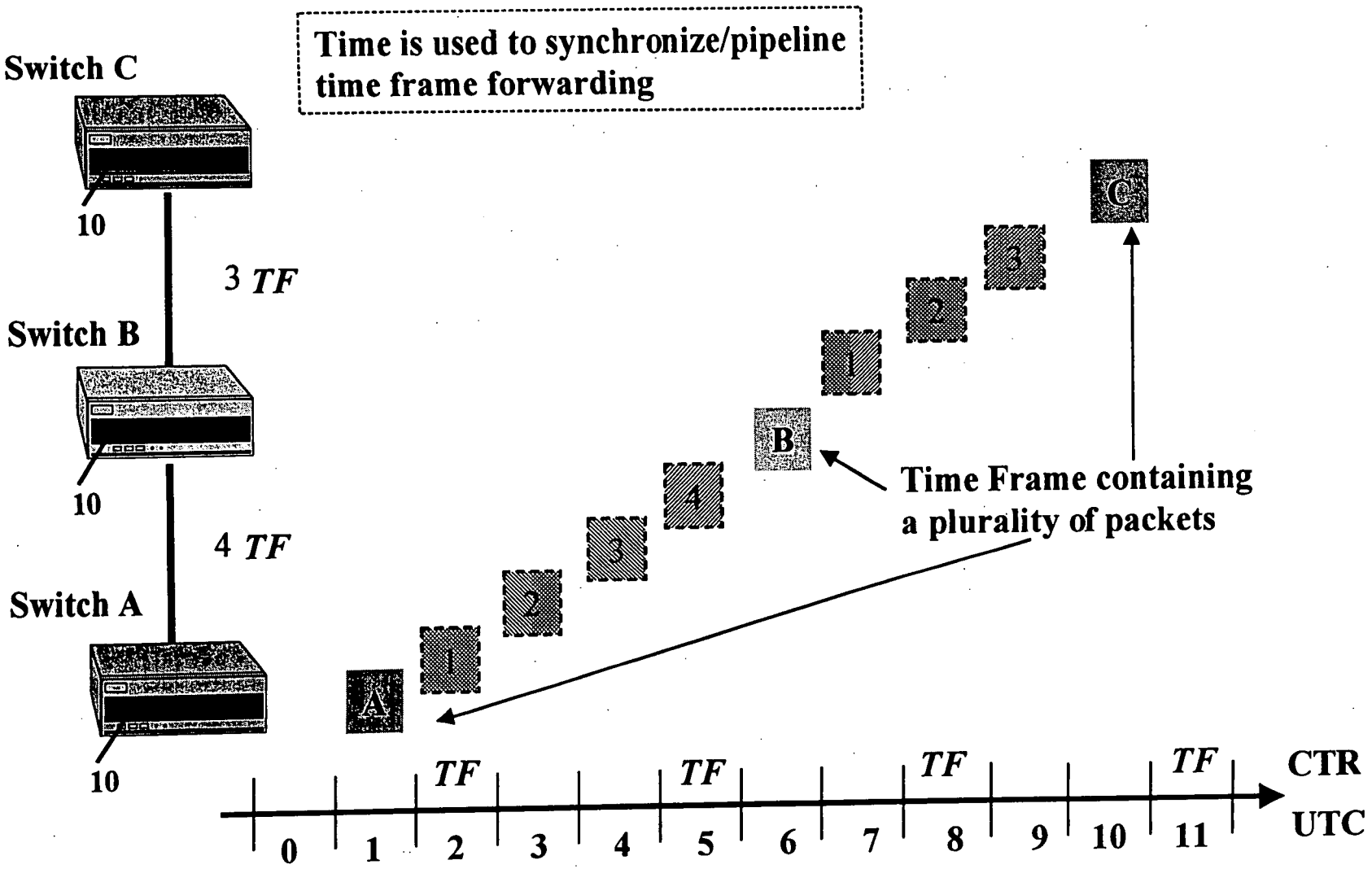

Time is used to synchronize/pipeline time frame forwarding
Switch C
10
3 TF
Switch B
10
4 TF
Switch A
10
A
1
2
3
4
B
1
2
3
C
Time Frame containing a plurality of packets
TF
TF
TF
TF
CTR
UTC
0
1
2
3
4
5
6
7
8
9
10
11

FIG. 29

2900

WDM basic property:
The source of <u>any wavelength</u> (W1, W2, and W3) in <u>any time frame</u> can come from <u>any input port</u>, $1 <= i,j,k,l,m,n,o,p,q <= N$.

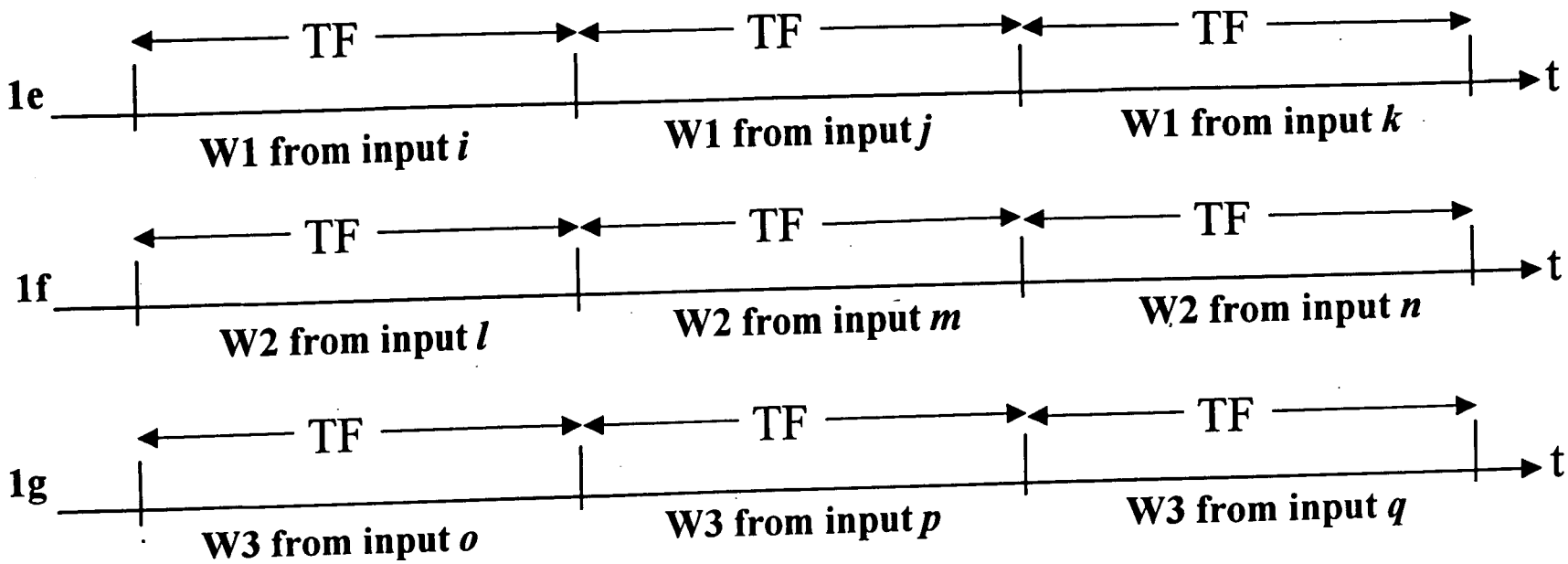


FIG. 30

Optical switching & forwarding of time frames

Mapping: *(p-in,w-in, t-in,c-in)* TO *(p-out,w-out,t-out,c-out)*

3010

p-in - input port #
w-in - input wavelength (color)
t-in - time frame # in (within a time cycle)
c-in - time cycle # in (within a super cycle)

3020

p-out - output port #
w-out - output wavelength (color)
t-out - time frame # out (within a time cycle)
c-out - time cycle # out (within a super cycle)

Basic principle: **In every time frame within a time cycle and within a super cycle, an input wavelength is switched to a selected defined subset of out-going optical channels**

3030

Table for a given: *w-in* and *p-in*

Super cycle with 4 time cycles

Time cycle with 4 time frames

	c-in-1	*c-in-2*	*c-in-3*	*c-in-4*
t-in-1				
t-in-2			***p-out,w-out t-out,c-out***	
t-in-3				
t-in-4				

3000

FIG. 31

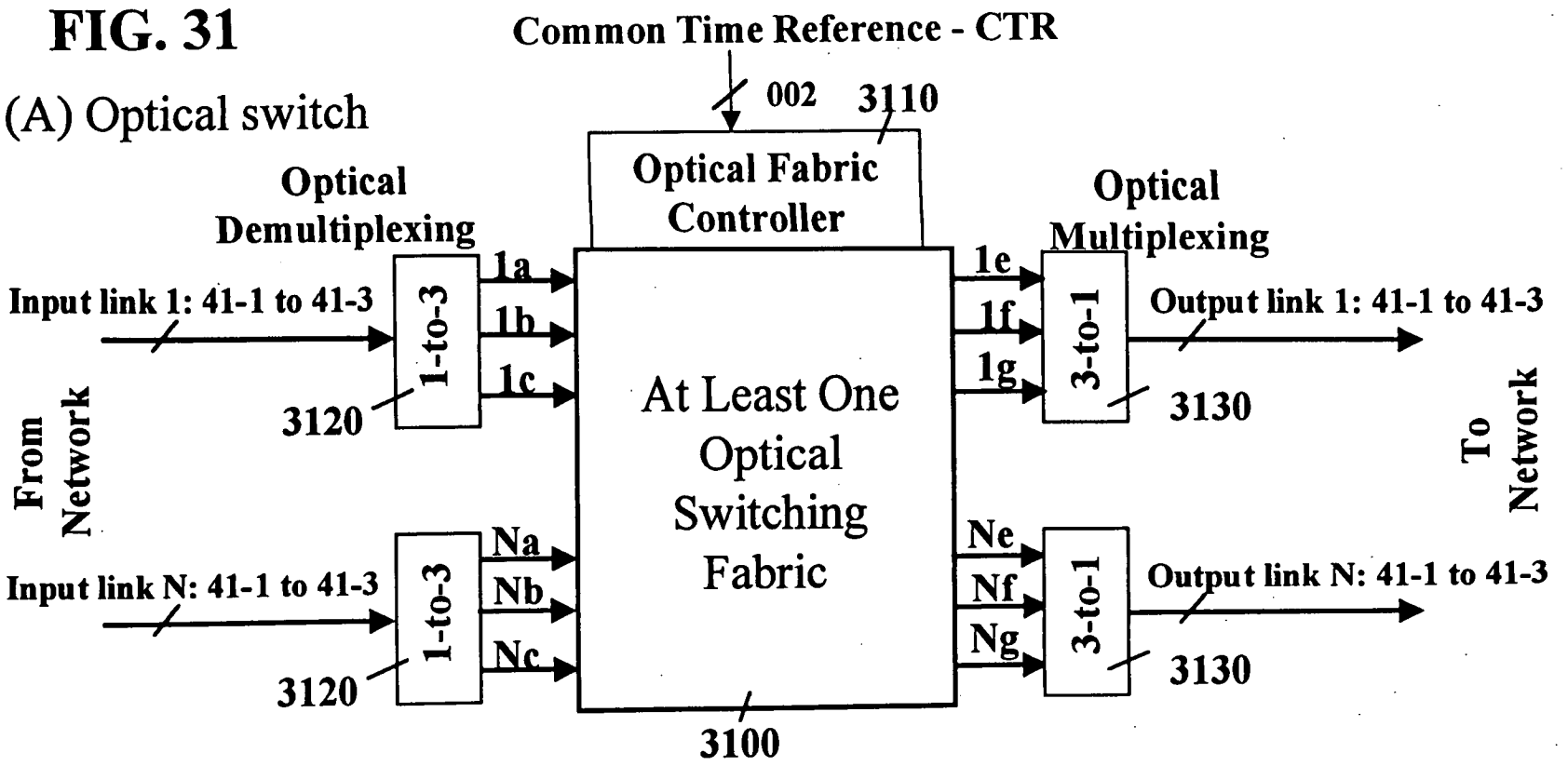


FIG. 32

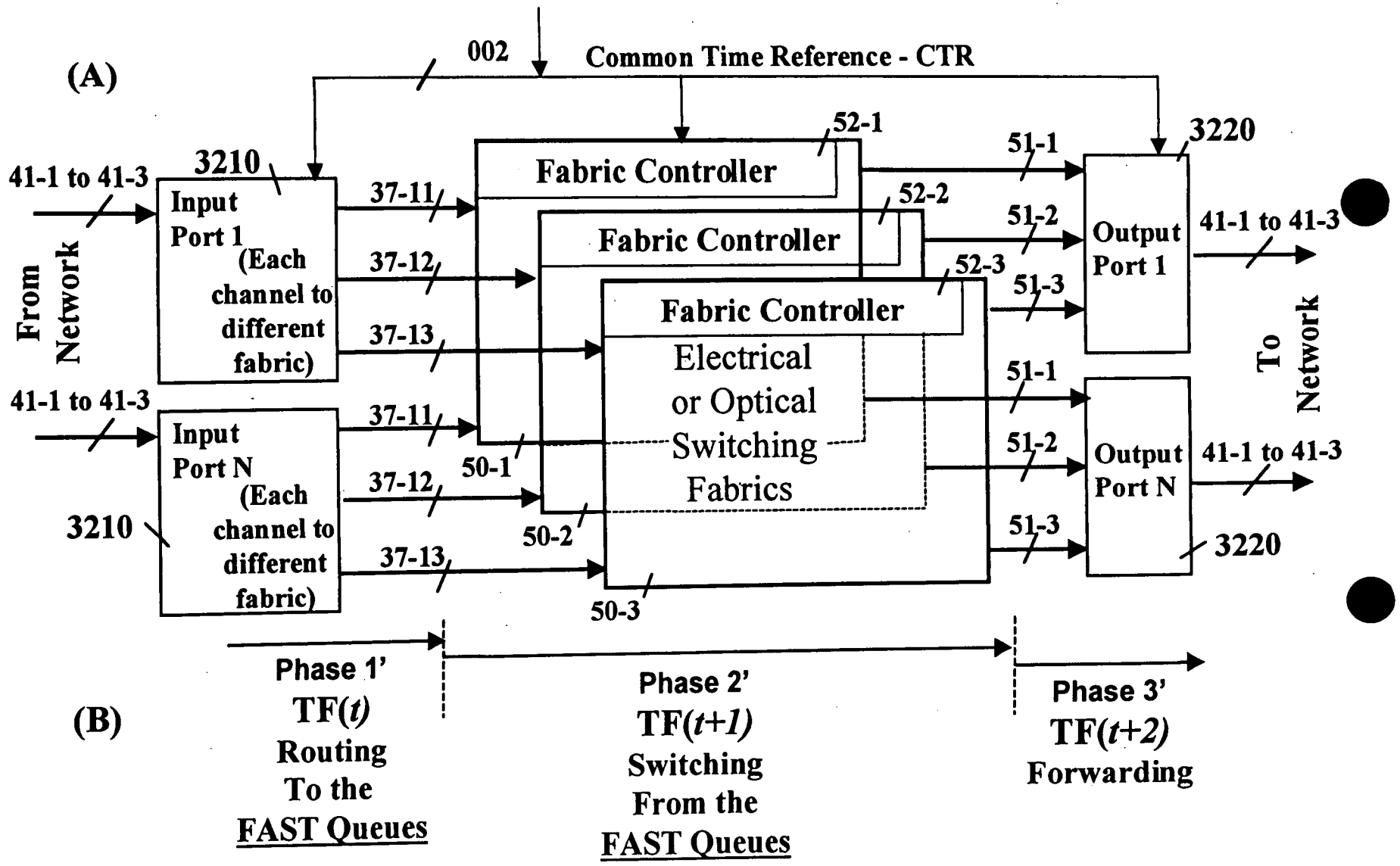

(A)
002
Common Time Reference - CTR
41-1 to 41-3
3210
Input Port 1 (Each channel to different fabric)
From Network
41-1 to 41-3
Input Port N (Each channel to different fabric)
3210
37-11
37-12
37-13
37-11
37-12
37-13
Fabric Controller
52-1
Fabric Controller
52-2
Fabric Controller
52-3
Electrical or Optical Switching Fabrics
50-1
50-2
50-3
51-1
51-2
51-3
51-1
51-2
51-3
3220
Output Port 1
41-1 to 41-3
To Network
Output Port N
41-1 to 41-3
3220
(B)
Phase 1'
TF(t)
Routing
To the
FAST Queues
Phase 2'
TF(t+1)
Switching
From the
FAST Queues
Phase 3'
TF(t+2)
Forwarding

FIG. 33

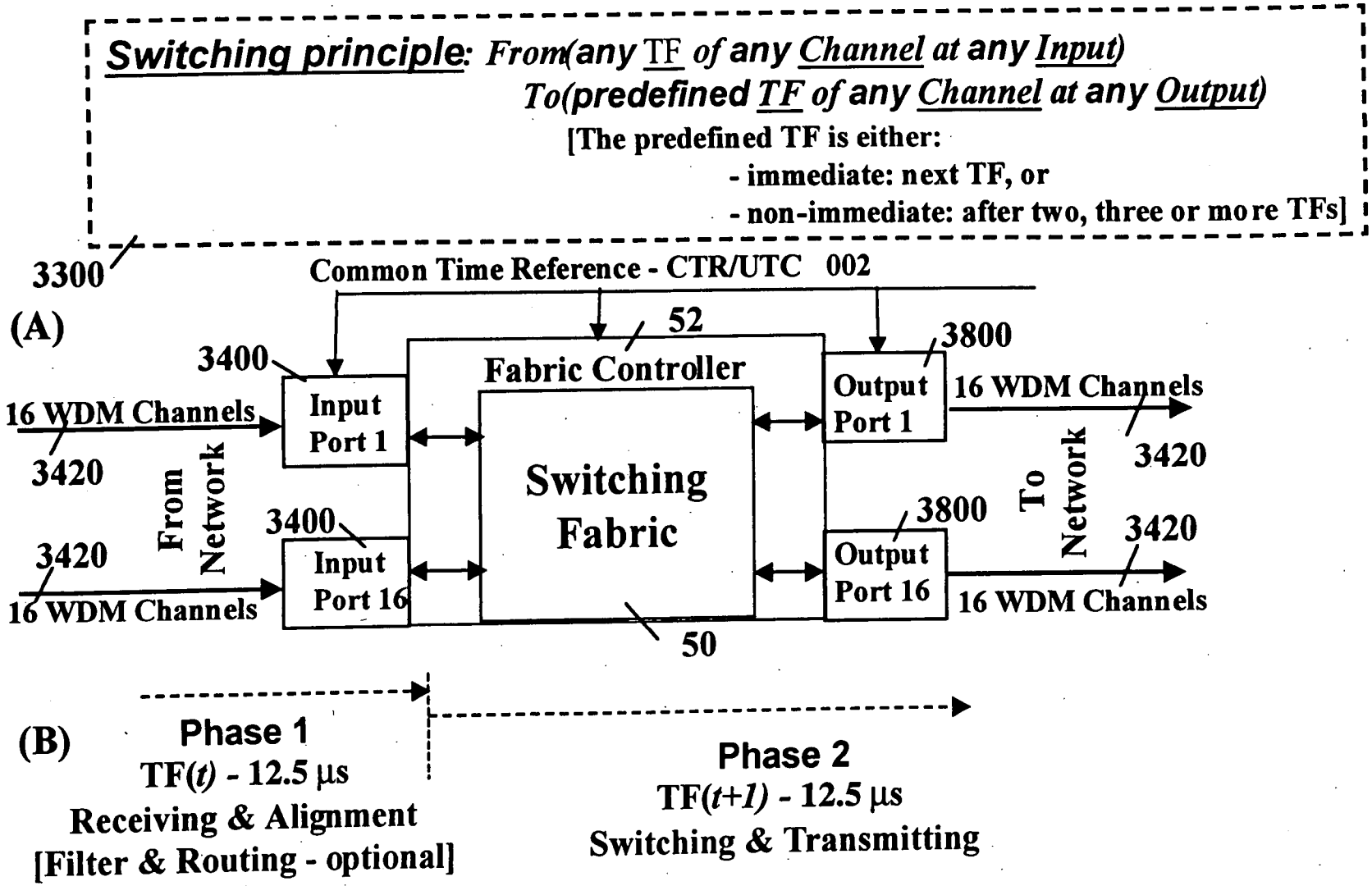

Switching principle: From(any TF of any Channel at any Input)
To(predefined TF of any Channel at any Output)
[The predefined TF is either:
- immediate: next TF, or
- non-immediate: after two, three or more TFs]
3300
(A)
Common Time Reference - CTR/UTC 002
52
Fabric Controller
3400
Input Port 1
16 WDM Channels
3420
From Network
3400
Input Port 16
3420
16 WDM Channels
Switching Fabric
50
3800
Output Port 1
16 WDM Channels
3420
To Network
3800
Output Port 16
3420
16 WDM Channels
(B)
Phase 1
TF(t) - 12.5 µs
Receiving & Alignment
[Filter & Routing - optional]
Phase 2
TF(t+1) - 12.5 µs
Switching & Transmitting

FIG. 34

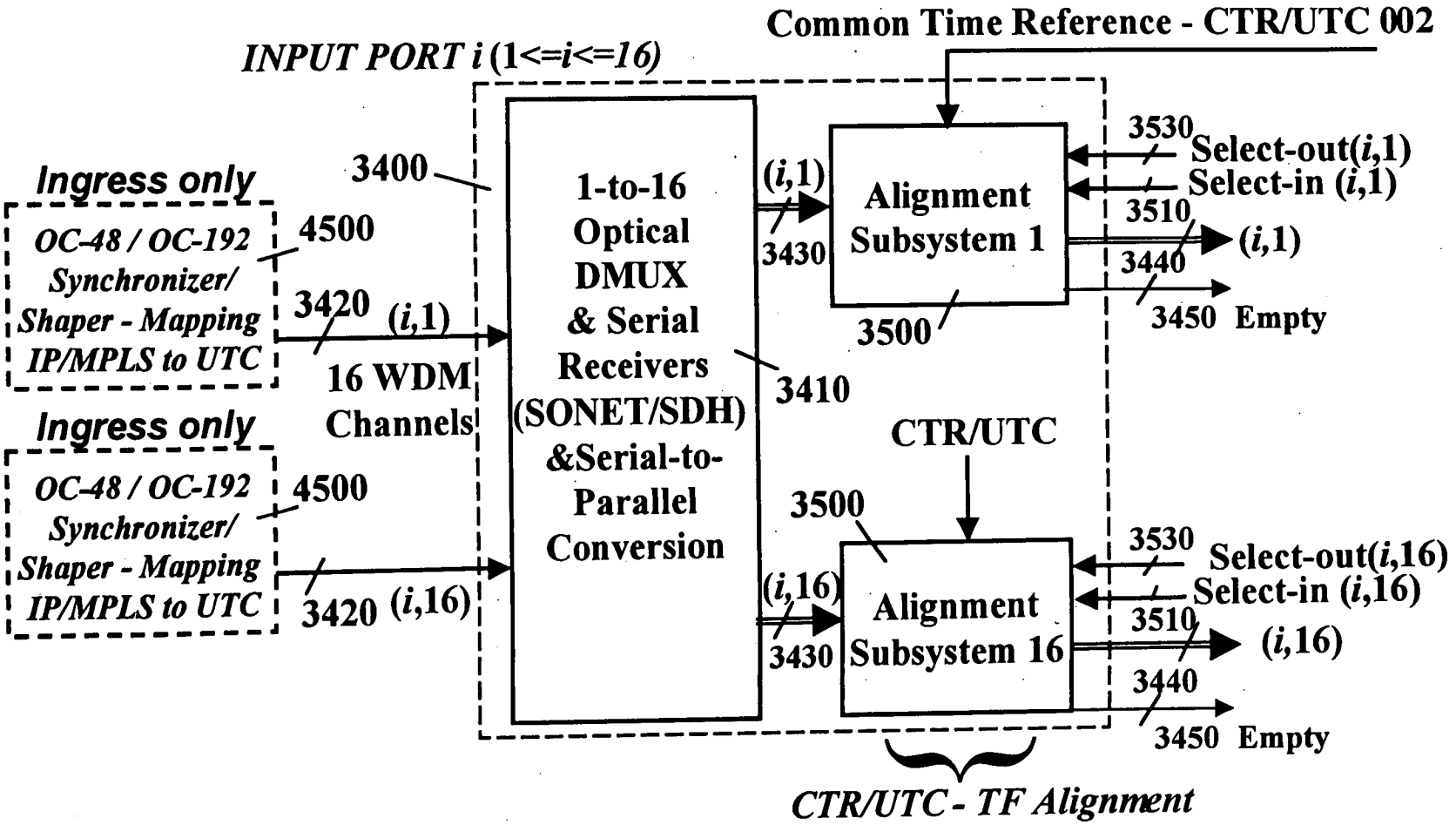
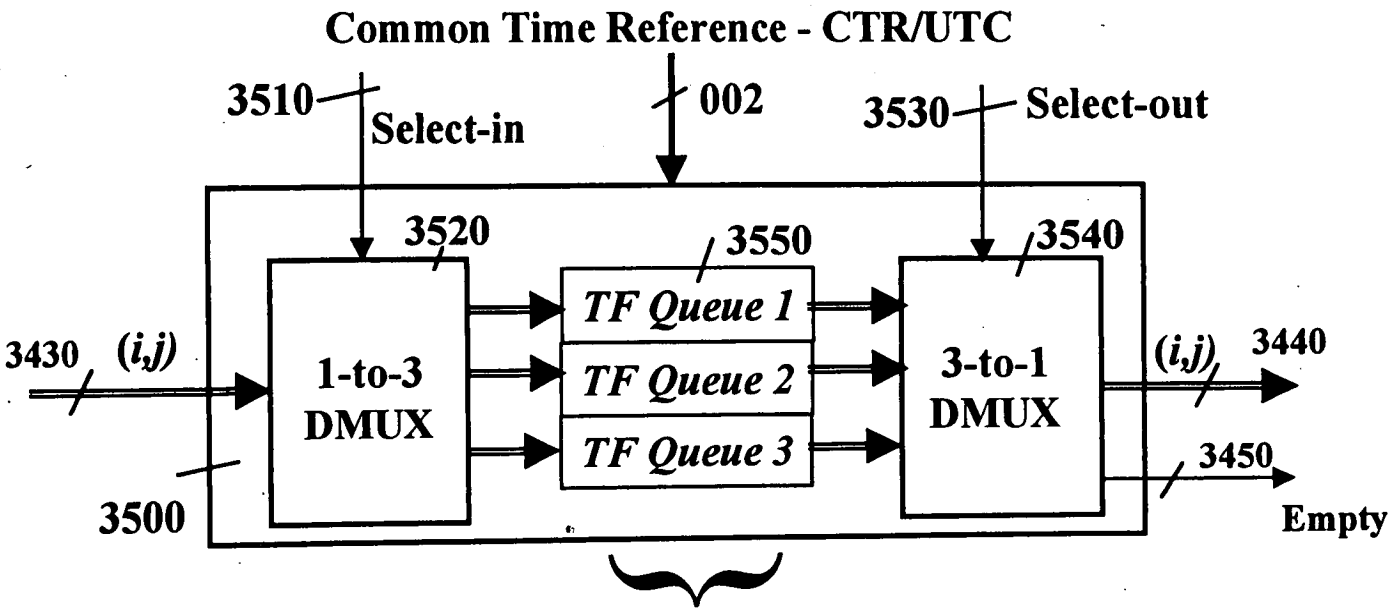


FIG. 35



Alignment Subsystem for Channel *j* at Input Port *i*
with a Plurality of Time Frame Queues

FIG. 36

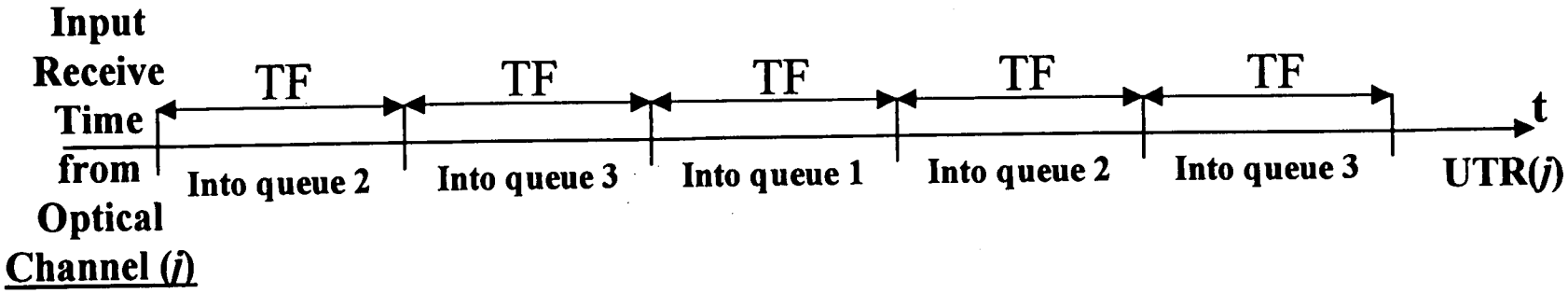
3600

***TF Alignment of* UTR(j) *to* UTC - with three input queues - principle of operation:**

The same queue is not used simultaneously for:

1. Receiving data packets from the serial link, and

2. Forwarding data packets to the switch



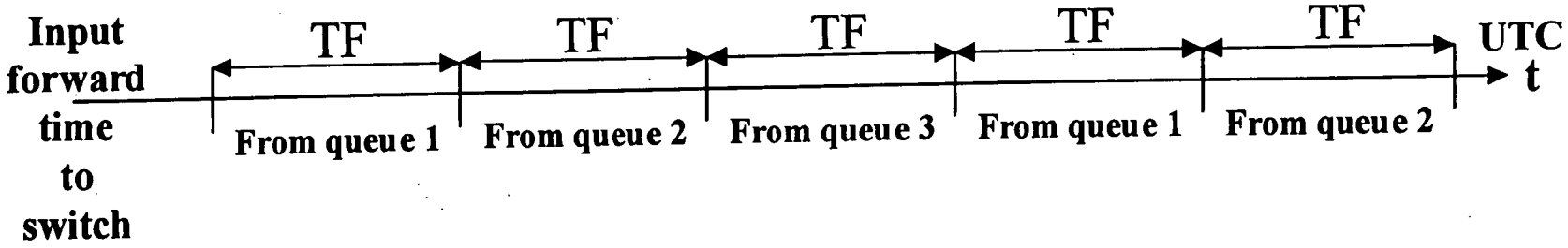
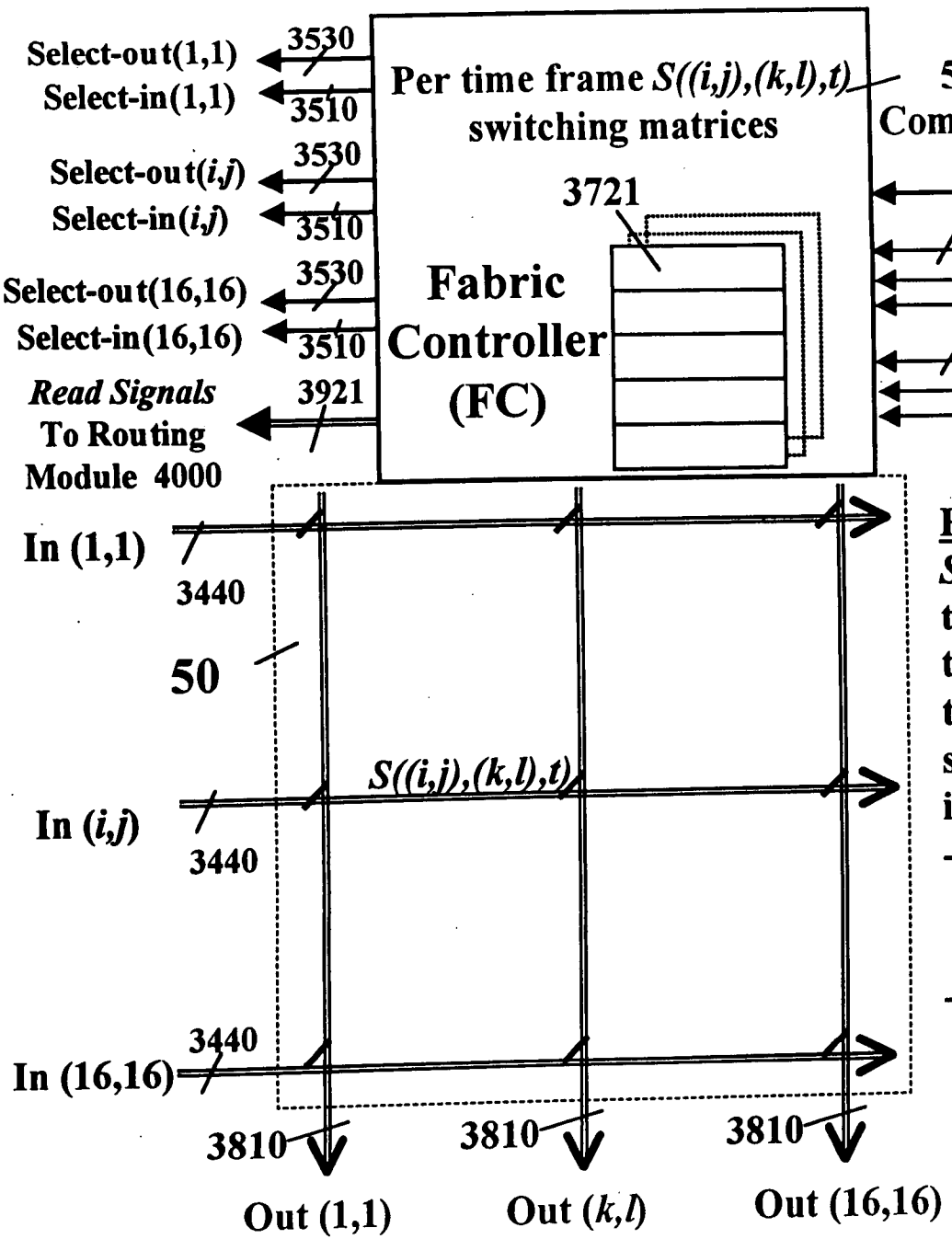


FIG. 37



Fabric controller (FC):

S ((i,j),(k,l),t) **- switching matrix for every time frame in each time cycle and super cycle, the matrix defines which input channel *i,j* should be connected to output channel *k,l* - in time frame *t*, where *S ((i,j),(k,l),t)=1:***

- **1. At every time frame an input channel can be connected to one or more output optical channels (multicast - MCST)**
- **2. At every time frame an output optical channel can be connected to at most one input optical channel**

FIG. 38

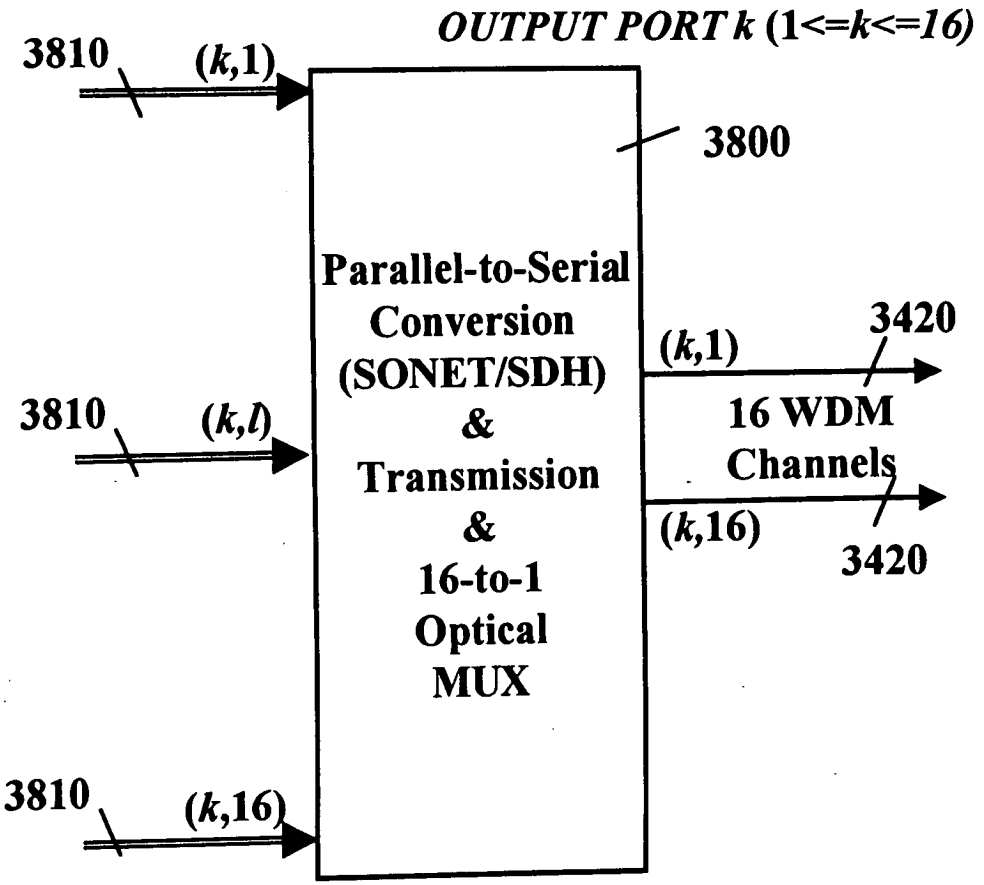


FIG. 39

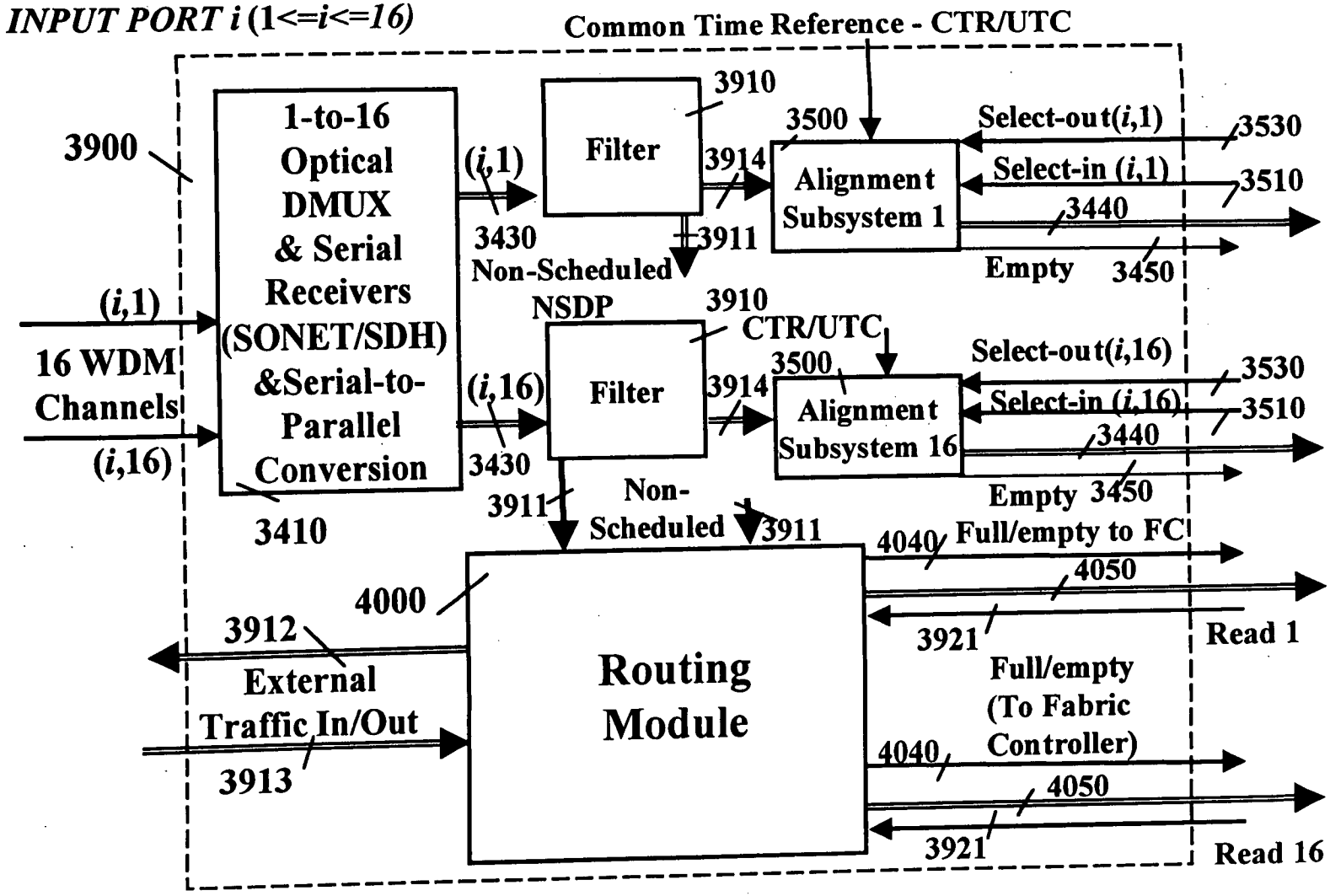


FIG. 40

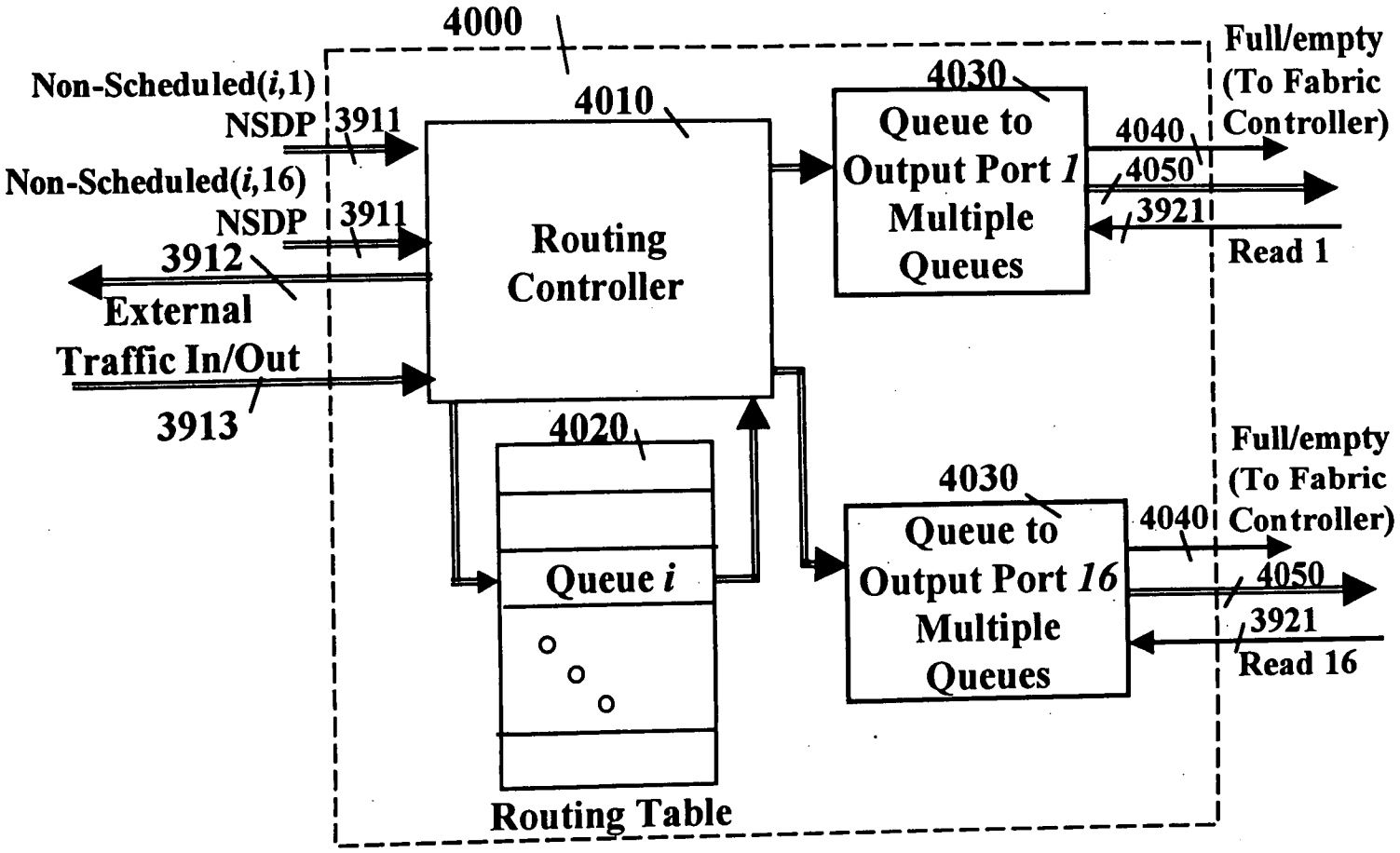


FIG. 41

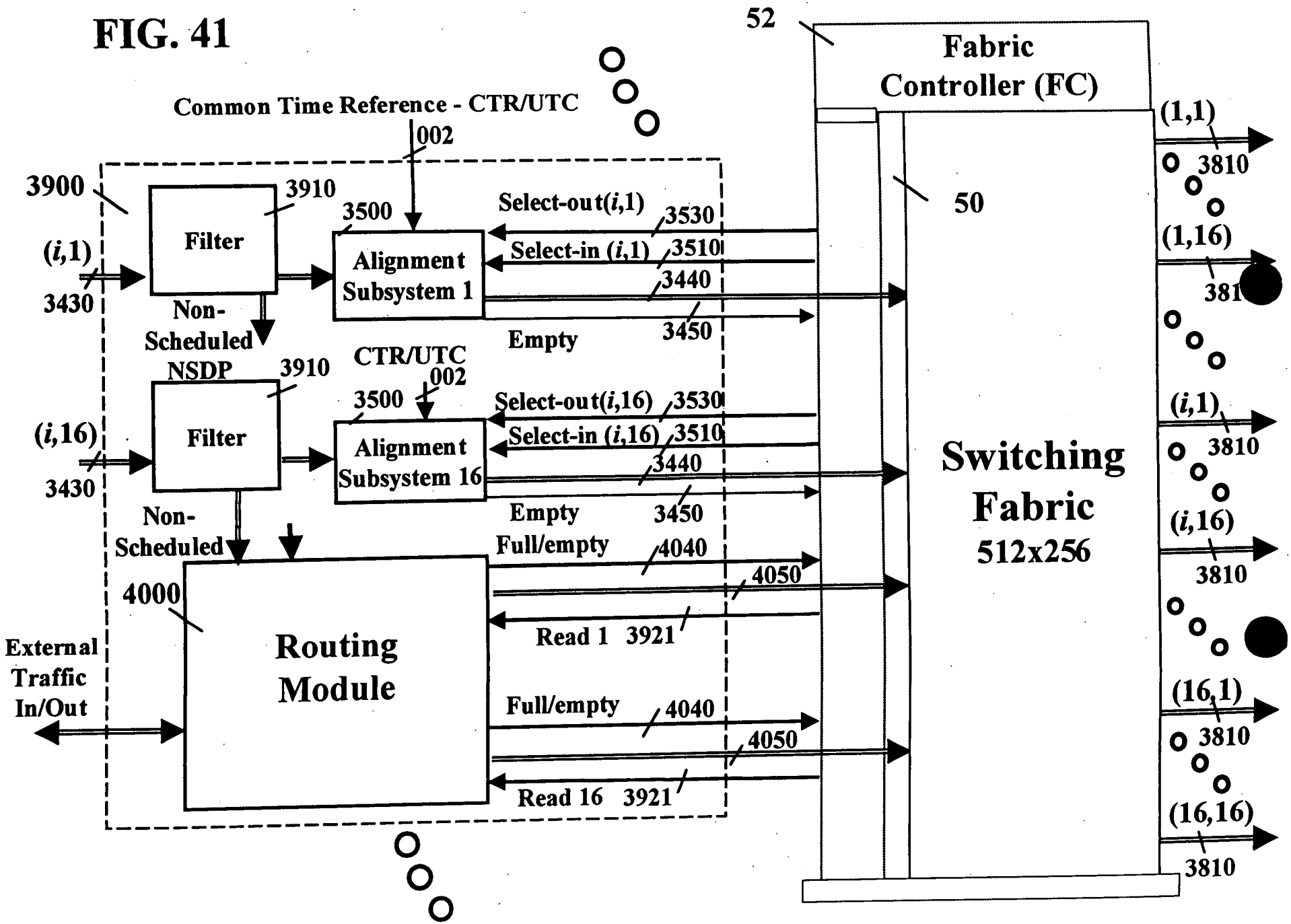

52
Fabric Controller (FC)
Common Time Reference - CTR/UTC
002
3900
3910
Filter
3500
Alignment Subsystem 1
Select-out(i,1)
3530
Select-in (i,1)
3510
3440
Empty
3450
(i,1)
3430
Non-Scheduled
NSDP
CTR/UTC
002
Filter
Alignment Subsystem 16
Select-out(i,16)
Select-in (i,16)
(i,16)
Non-Scheduled
Full/empty
4040
4050
Read 1 3921
Read 16 3921
4000
Routing Module
External Traffic In/Out
50
Switching Fabric 512x256
(1,1)
(1,16)
(i,1)
(i,16)
(16,1)
(16,16)
3810

FIG. 42

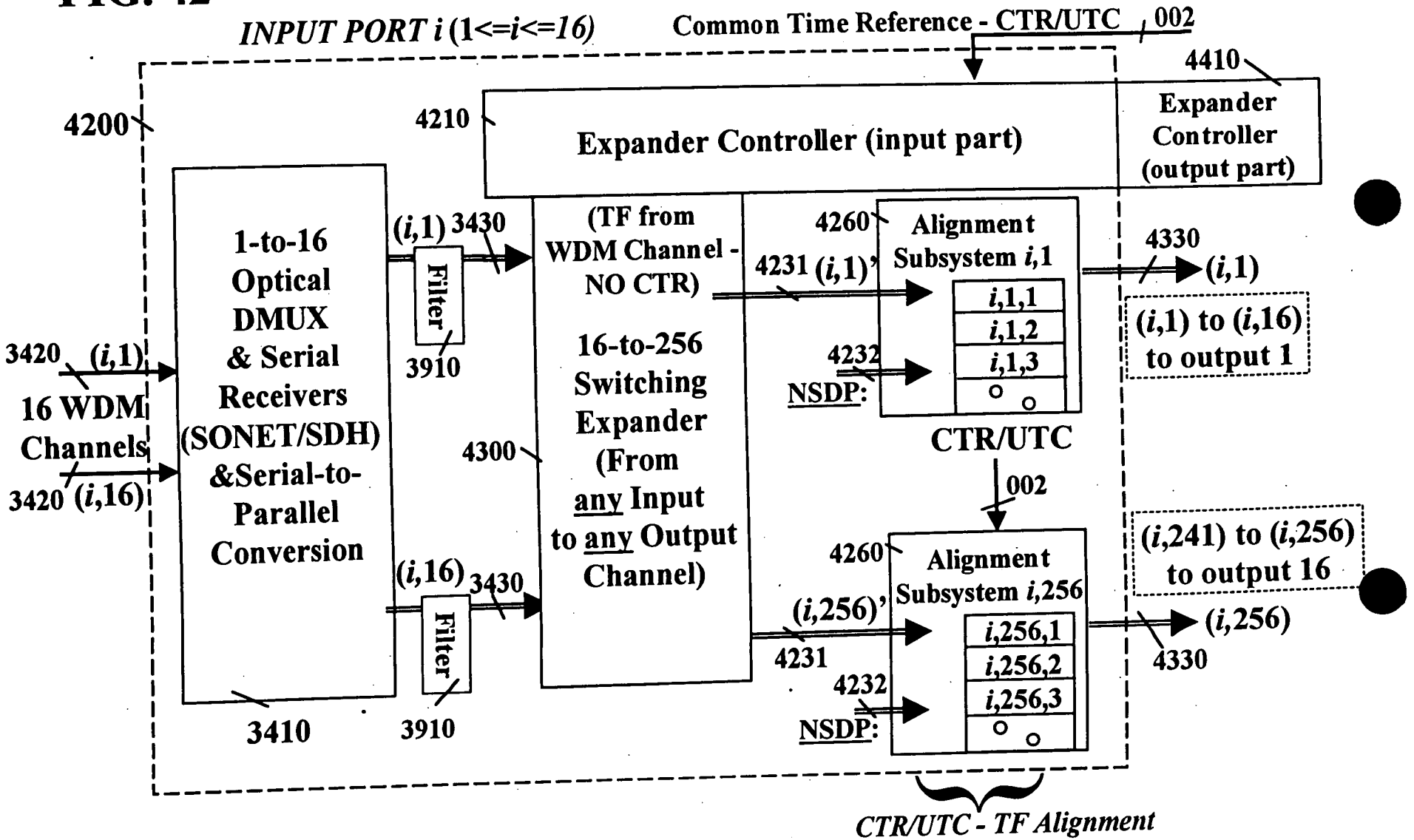
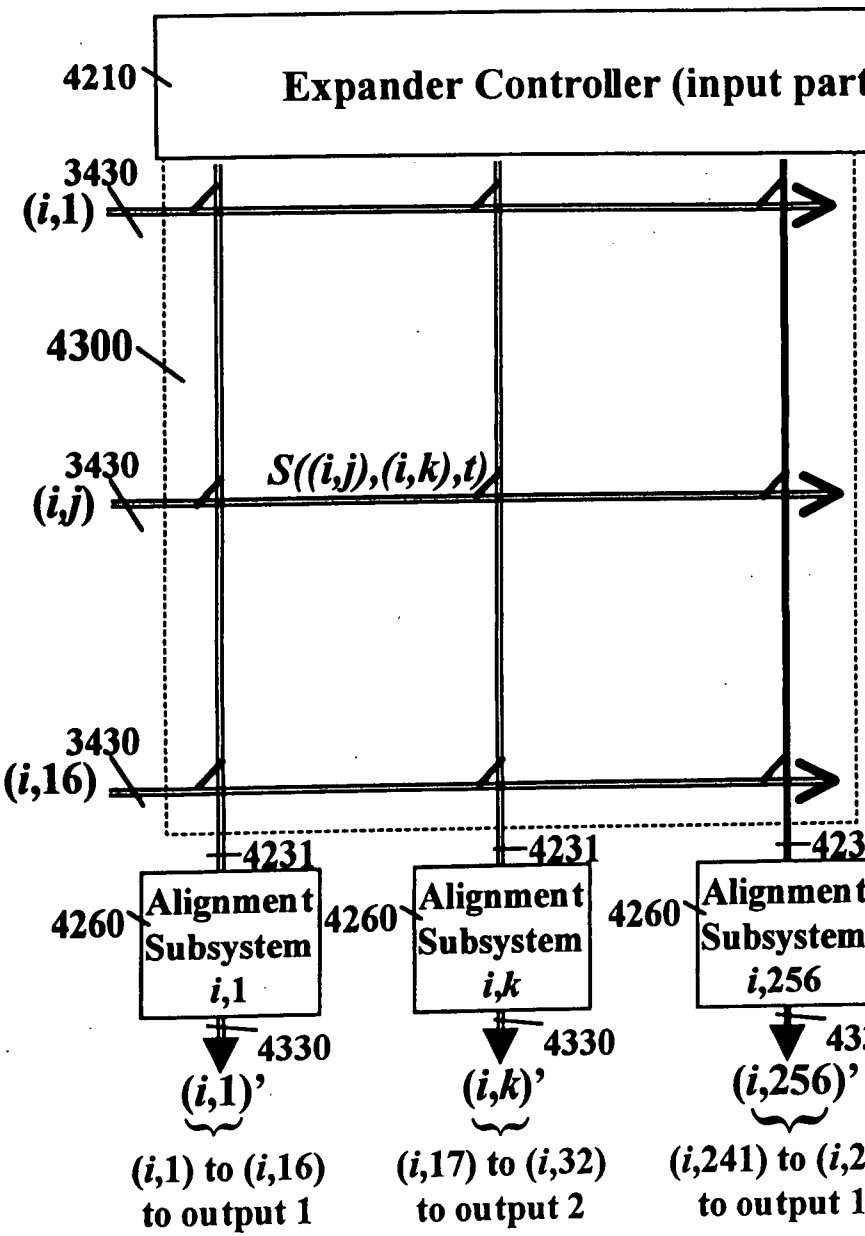

INPUT PORT i (1<=i<=16)
Common Time Reference - CTR/UTC
002
4200
4210
Expander Controller (input part)
4410
Expander Controller (output part)
1-to-16 Optical DMUX & Serial Receivers (SONET/SDH) &Serial-to-Parallel Conversion
3410
(i,1) 3430
Filter
3910
(i,16) 3430
Filter
3910
3420 (i,1)
16 WDM Channels
3420 (i,16)
(TF from WDM Channel - NO CTR)
16-to-256 Switching Expander (From any Input to any Output Channel)
4300
4260
Alignment Subsystem i,1
4231 (i,1)'
i,1,1
i,1,2
i,1,3
4232
NSDP:
CTR/UTC
002
4330
(i,1)
(i,1) to (i,16) to output 1
4260
Alignment Subsystem i,256
(i,256)'
4231
i,256,1
i,256,2
i,256,3
4232
NSDP:
4330
(i,256)
(i,241) to (i,256) to output 16
CTR/UTC - TF Alignment

FIG. 43



Expander controller - input port *i* (*ECi*):

S ((i,j),(i,k),t) **- switching matrix for every time frame in each time cycle and super cycle, the matrix defines which input *(i,j)* should be connected to output *(i,k)'* - in time frame *t*, where *S ((i,j),(i,k)',t)=1:***

- **1. At every time frame an input port can be connected to one or more output ports (multicast - MCST)**
- **2. At every time frame an output port can be connected to at most one input port**

The 1st line to the 1st selector - line *i*

.

.

The 16th line to the 16th selector - line *i*

FIG. 44

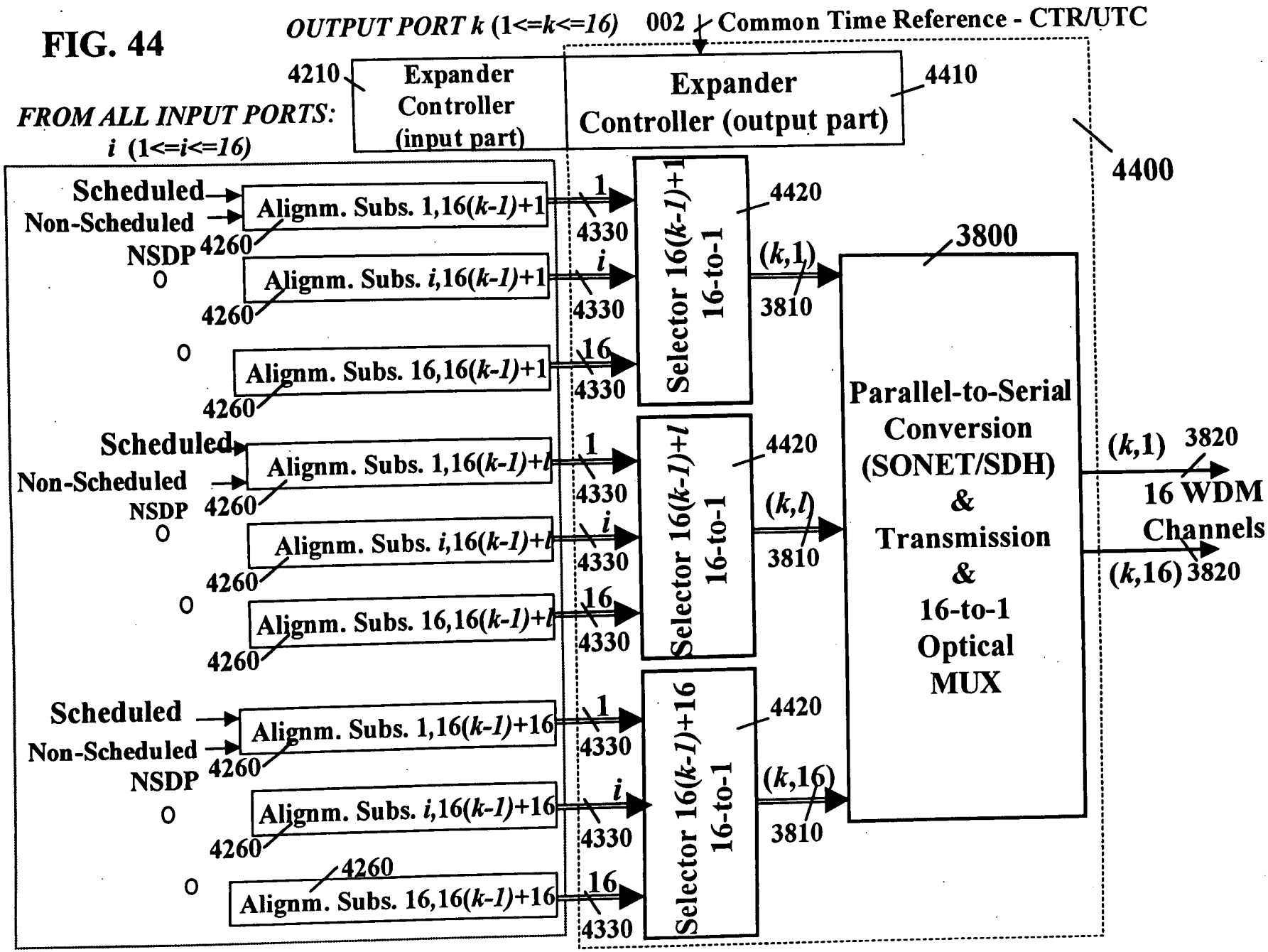


FIG. 45

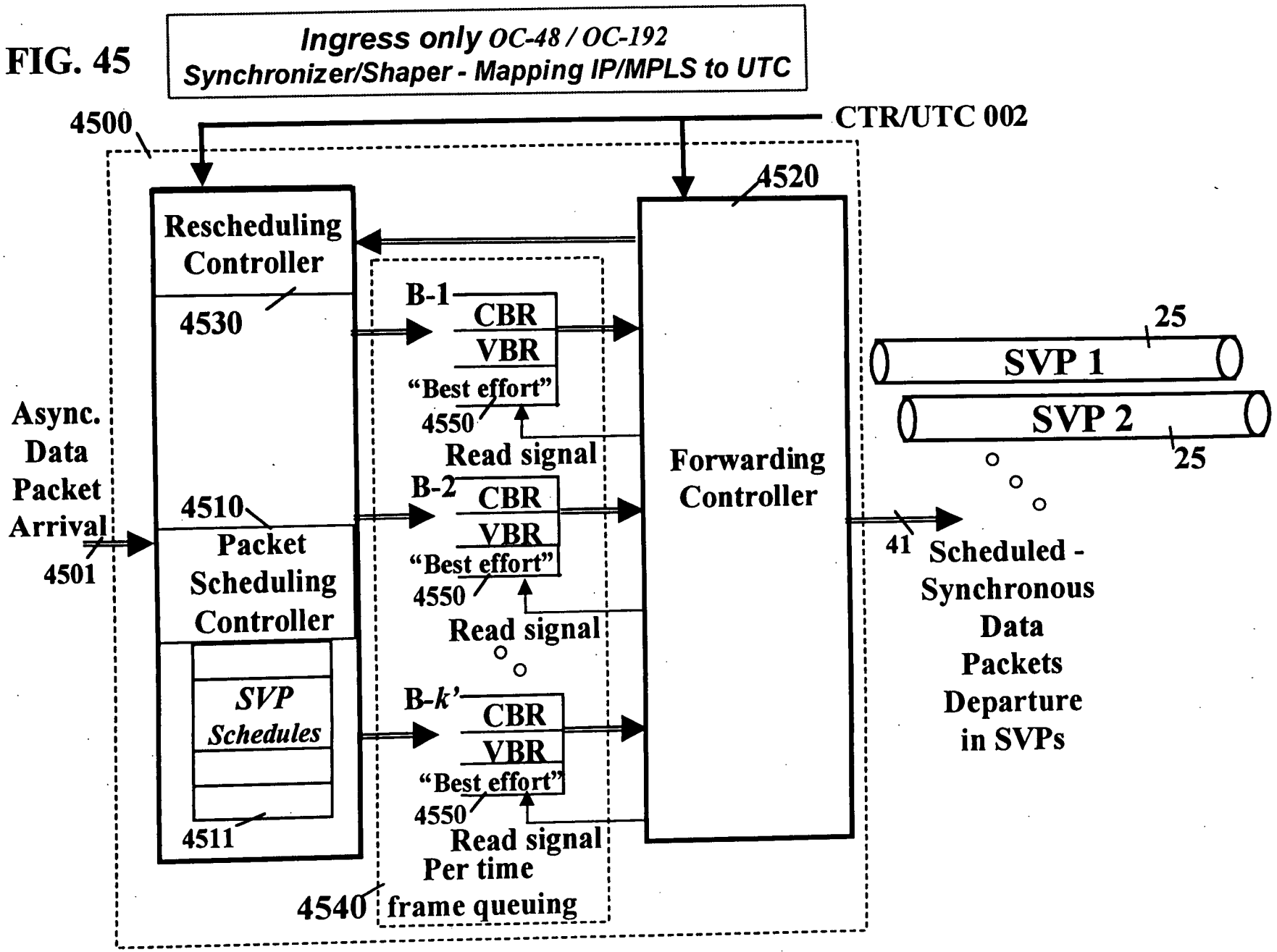


FIG. 46

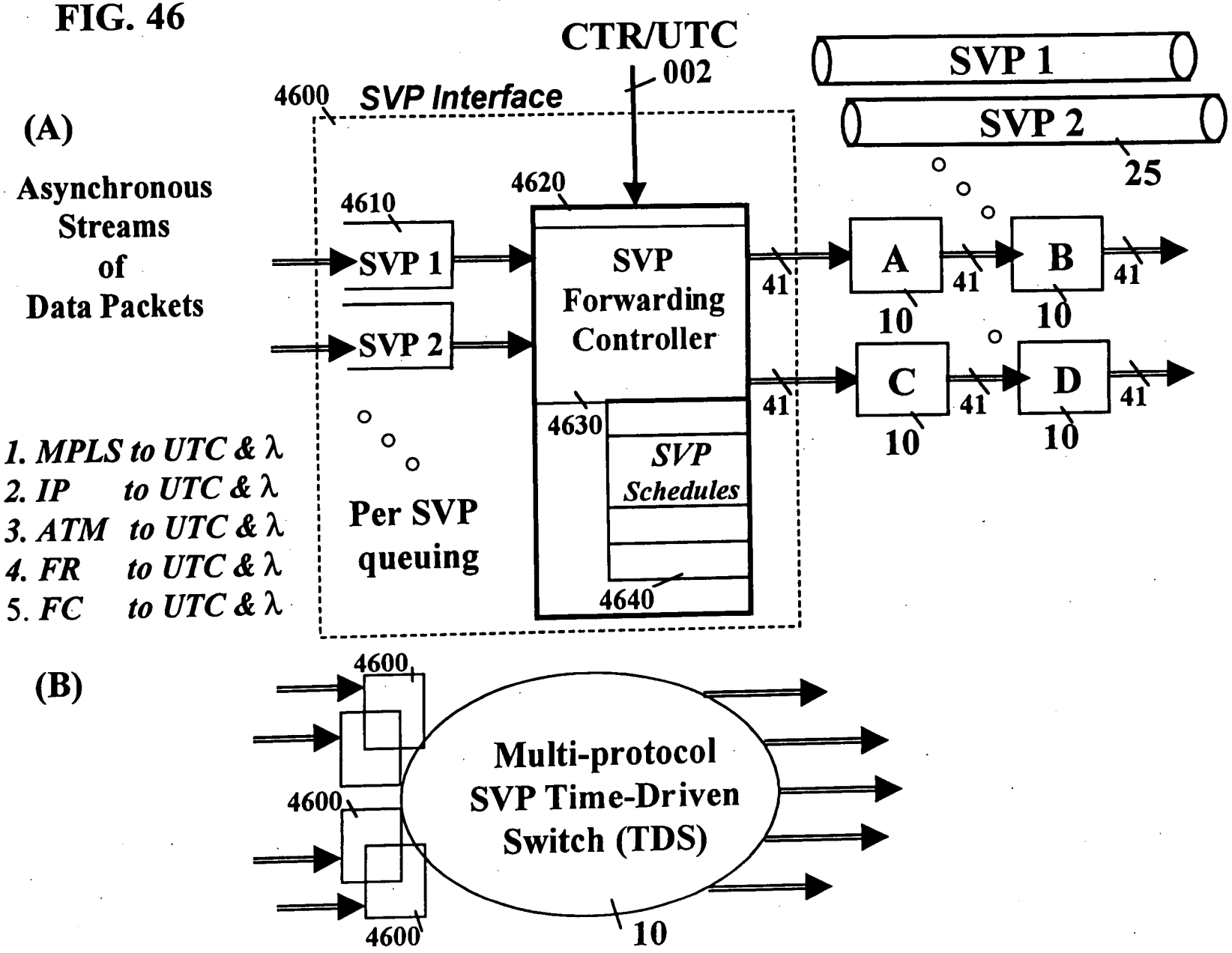


FIG. 47

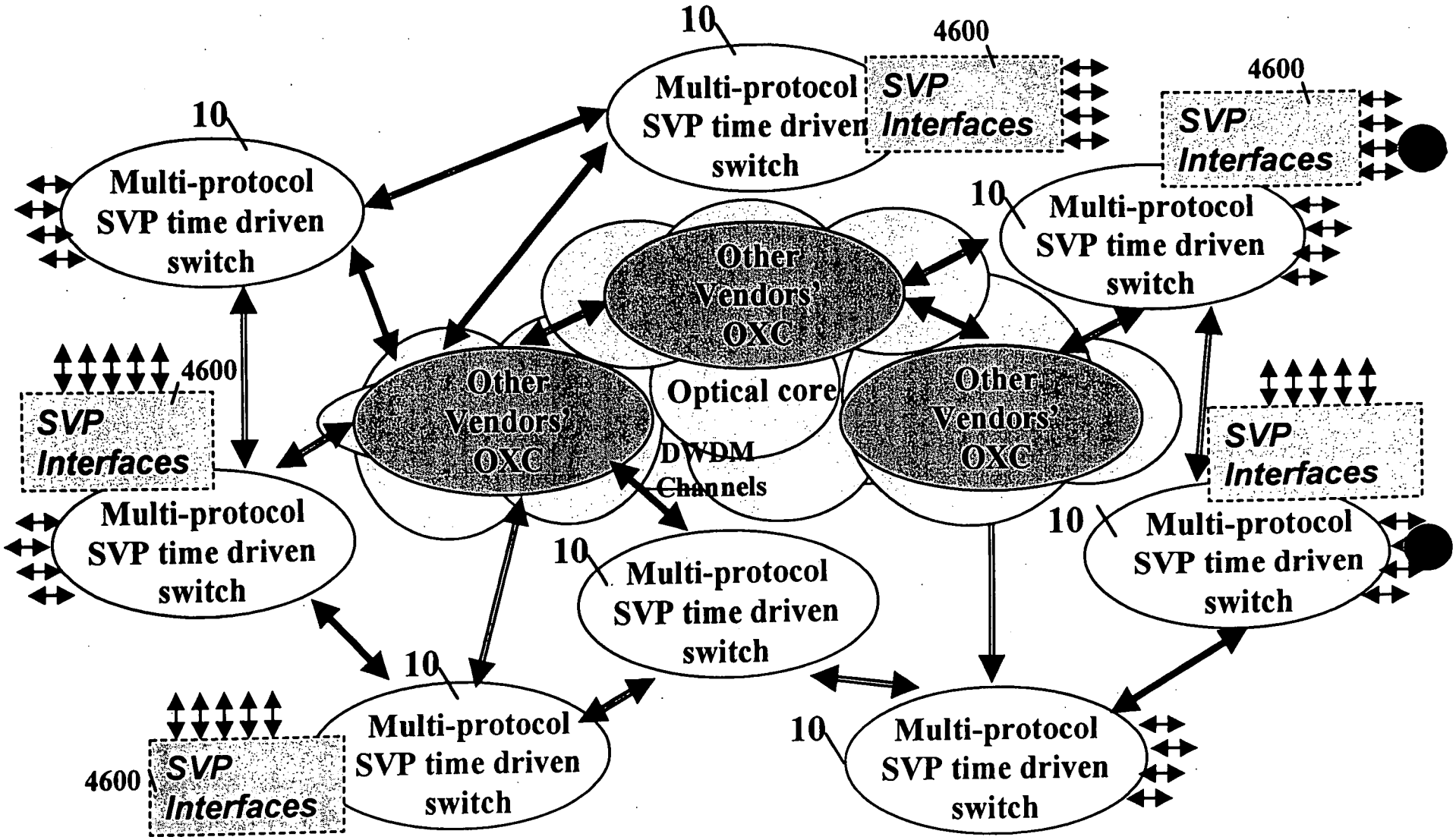

10
Multi-protocol SVP time driven switch
4600
SVP Interfaces
Other Vendors' OXC
Optical core
DWDM Channels

FIG. 48

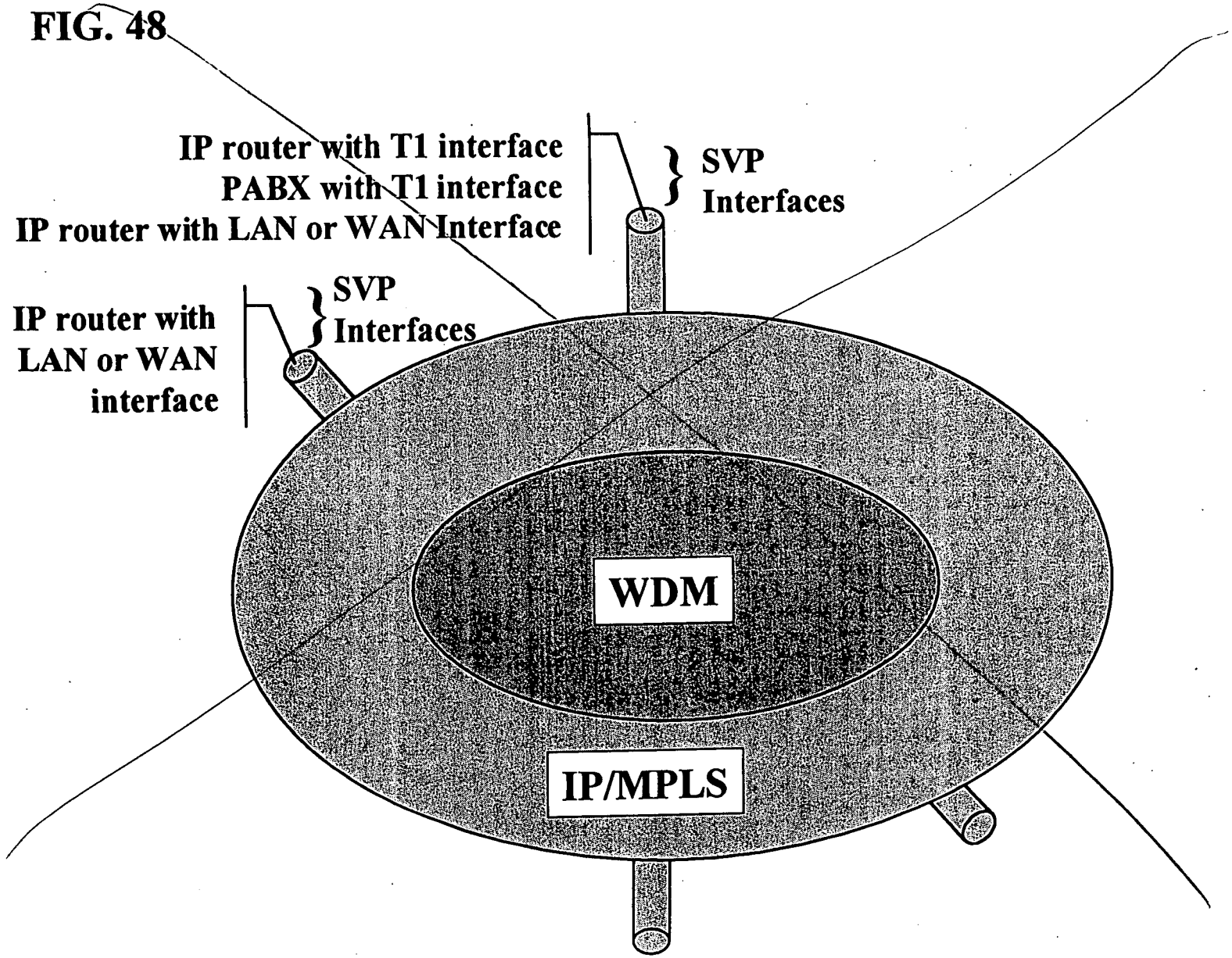


FIG. 49

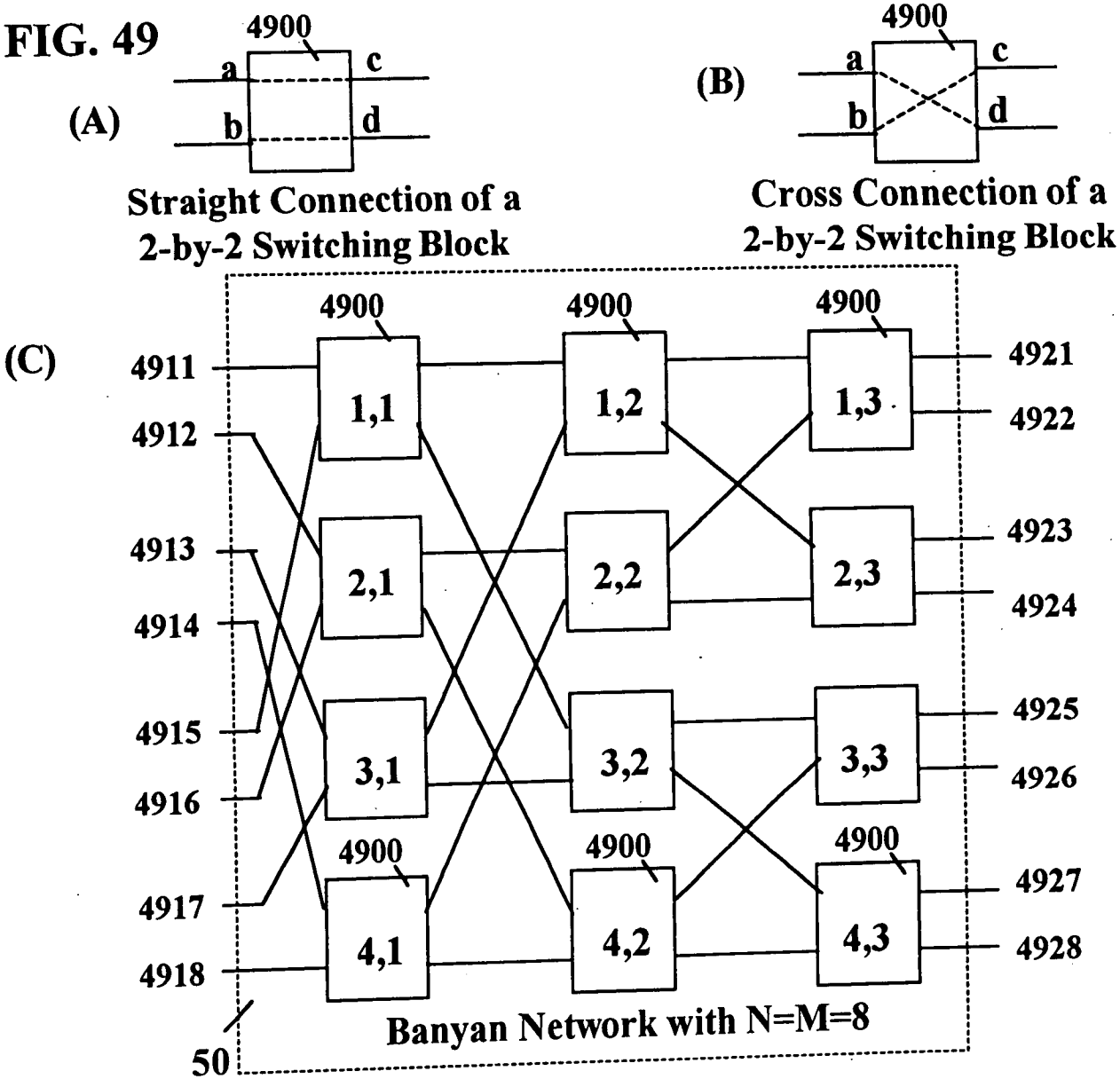


FIG. 50

(A)

Switching elements	Multistage $a*N*\lg_a N$	Crossbar N^2
For N=256, a=4	4K	64K
For N=1024, a=4	20K	1,000K

(B)